Evaluation Board

EP440xC 1.1 (DES0211)
AMCC Sequoia and Rainier
User Manual

Technical Support:
sequoiasupport@amcc.com
rainiersupport@amcc.com

P5010000069SB01

Copyright

Notice

Embedded Planet, LLC., reserves the right to modify the information contained herein as necessary. Embedded Planet assumes no responsibility for any errors which may appear in this document. Information in this document is provided solely to enable system and software implementers to use Embedded Planet products.

This manual in whole or in part, is to be considered the intellectual property of Embedded Planet. This document is intended for the sole purpose of the owner of an Embedded Planet product. Neither the document, nor reproductions of it, nor information derived from it is to be given to others, nor used for any other purpose other than for development of Embedded Planet computing engine applications, by original, authorized owners of Embedded Planet products.

Trademarks

Embedded Planet, Linux Planet, Blue Planet, RPX LITE, and RPX LICC are trademarks or registered trademarks of Embedded Planet.

PowerPC is a trademark of International Business Machines, Inc.

AMCC is a registered trademark of Applied Micro Circuits Corporation.

Spansion and MirrorBit are trademarks of Spansion, LLC.

Infineon is a trademark of Infineon Technologies AG.

Wind River Systems, VxWorks, and Tornado are registered trademarks of Wind River Systems, Inc.

All other names and trademarks are the property of their respective owners and are hereby acknowledged.

Contents

Contents (continued)

List of Figures

List of Tables

List of Tables (continued)

List of Tables (continued)

Introduction

Chapter 1

This document describes the EP440xC board from Embedded Planet that is included in evaluation kits for the AMCC PowerPC 440EPx and 440GRx processors.

The Embedded Planet 440xC board is intended for evaluating the PPC440EPx and PPC440GRx processors, as well as for general-purpose, embedded application development. The PPC440EPx and PPC440GRx processors combine the PowerPC 440 core together with an extensive set of peripherals and I/O controllers.

Functions

The functions included on the evaluation board are listed in Table 1-1.

Table 1-1. Hardware Features

Entity	Function
Processor	PPC440EPx (up to 667 MHz) or PPC440GRx (up to 667 MHz)
DDR2 SDRAM	256 MBytes, 333 MHz data rate, 64-bit bus width
NOR FLASH	64 MBytes, 16-bit bus width
NAND FLASH	32 MBytes, 8-bit bus width
Ethernet port	RGMII0 - 10BaseT/100BaseTX/1000BaseT (RJ-45)
	RGMII1 - 10BaseT/100BaseTX/1000BaseT (RJ-45)
Serial port (RS-232)	UART0 - 4-wire interface (DB-9)
	UART1 - 4-wire interface (DB-9)
PCI	Dual PCI edge slot 33 MHz or 66 MHz per PCI Local Bus 2.2 specification Host only +3.3VDC signaling
USB[1]	USB0 - USB 2.0 device with UTMI (SMSC GT3200)
	USB1 - USB 2.0 host
	USB2 - USB 2.0 device
Serial EEPROM	I2C0 - 512 Bytes (2), 1 x 5 header
Serial temperature sensor	I2C0 - 10-bit, 0.25^{o} C temperature resolution
I2C / SPI	I2C1 - 1 x 5 header
Debug	JTAG/CPU - 2 x 8 header
	JTAG/CPLD - 2 x 5 header
	TRACE - 38 Tyco Mictor connector

Table 1-1. Hardware Features *(continued)*

Entity	Function
Switches	4-position slide configuration switch read via CPLD for board configuration (factory set; should not be changed)
	4-position slide user switch read via CPLD status register
	Push-button reset switch
LEDs	Power, status, reset, 2-user programmable via control register
+5 VDC supply[2]	Single +5 VDC power supply source
Operating temperature	0° C to 70° C (32° F to 158° F)
BCSR	Board control and status registers

NOTES:
1. Not available for the PPC440GRx processor.
2. The means of disconnection from the mains power supply is the plug.
3. No serviceable parts.

How to Use This Manual

1. Refer to Chapter 2 for a description of the board features and functions.

2. Refer to Chapter 3 for a description of the connectors and headers available on the board.

3. Refer to Chapter 4 for a description of the LED indications for the board and Ethernet port.

4. Refer to Chapter 5 for board control and status register (BCSR) programming information.

5. Refer to Chapter 6 for hardware specific register and memory settings required for proper operation of the board.

6. Refer to Chapter 7 for programming information for the onboard I2C devices.

7. Refer to Chapter 8 for information about the possible interrupts.

About Embedded Planet

Embedded Planet is a leading single board computer and embedded systems solution provider. Our capabilities range from standard off the shelf single board computer products and embedded operating systems to full custom design and intellectual property solutions.

In 1997, Embedded Planet pioneered the Design, Develop, Deploy process for embedded systems engineering. This process allows our customers to take advantage of production tested, reusable product designs in all phases of system development to reduce time to market, project risk, and development costs.

Design

Embedded Planet products help remove risk and shorten the design cycle through production tested, integrated hardware and software designs. CPU module design is becoming more complicated with advanced memory interfaces and

highly integrated communications processors. Our production proven modules help OEMs eliminate the risky and time intensive design and verification of the CPU module and focus on their value added application.

Develop Embedded Planet products provide early access to production modules for all members of the engineering team to allow for a parallel development path. Software developers get access to turnkey platforms with the operating system of their choice ready to run out of the box. Hardware developers gain access to production designs and prototyping systems to test advanced system functionality. Fully integrated software and hardware platforms simplify and shorten the development cycle.

Deploy Embedded Planet products are ready to go to market today. Our designs are production proven and ready to be manufactured in quantity. We offer full lifecycle management to simplify the deployment of your embedded solution.

Document Conventions

This document uses standard text conventions to represent keys, display items, and user data inputs:

Display Item *Italic* - Identifies an item that displays on the screen such as a menu option or message (e.g., *File* > *Open*).

User Data Input **Bold** - Identifies any part of a command or user entry that is not optional or variable and must be entered exactly as shown.

Italic - Identifies any part of a command or user entry that is a variable parameter.

[ ] - Identifies any part of a command or user entry that is an optional parameter; text within the brackets follows the previously described conventions.

KEY - Identifies a specific key that is not alphabetic, numeric, or punctuation:

Press **ENTER**
Press **ESC V M** (press and release each key in sequence)
Press **CTRL-ALT-DEL (**press all keys in sequence simultaneously).

File Names `Name` - Indicates a file or directory name. Example:

```
file.h
/bin
```

Description

Chapter 2

This chapter provides some description of the evaluation board features including the PowerPC processor, external interfaces and firmware. Figure 2-1 is a simplified block diagram of the evaluation board. Figure 2-2 shows the top and bottom view board layouts. These figures show the headers unpopulated (i.e., ***without*** pins or connectors).

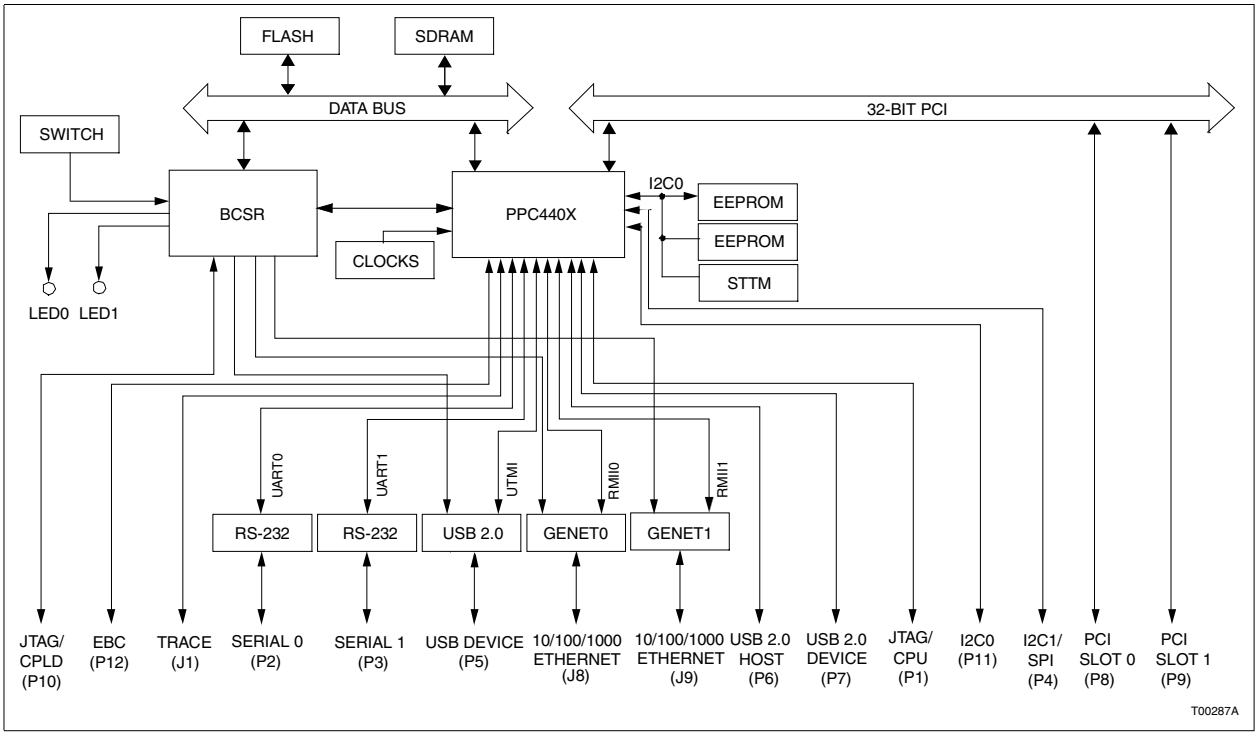

Figure 2-1. Simplified Block Diagram

PPC440EPx, PPC440GRx

Refer to ***PowerPC Processor*** in this chapter.

Clocking

The system clock is supplied from an Cypress CY22381FX programmable clock generator. The input to the CY22381FX device is a 22.1184 MHz oscillator. The CY22381FX device on the board provides the system clock input (SysClk) to the processor at 33.333 MHz. It also provides a 11.0592 MHz clock input to the UART baud rate generator and a 33 MHz clock input to the CPLD.

A Cypress CY2292F programmable clock generator provides clock signals to the remaining devices on the board. The input to the CY2292F device is a 12.000 MHz oscillator. During hard reset the board is configured for PCI asynchronous clocking mode. The M66EN signal enables either a 33 MHz or 66 Mhz clock signal for the CPU PCI clock and the PCI slot clock. The CY2292F device also provides a 25 MHz clock input to the 10/100/1000 Gigabit Ethernet devices, a 50 MHz clock

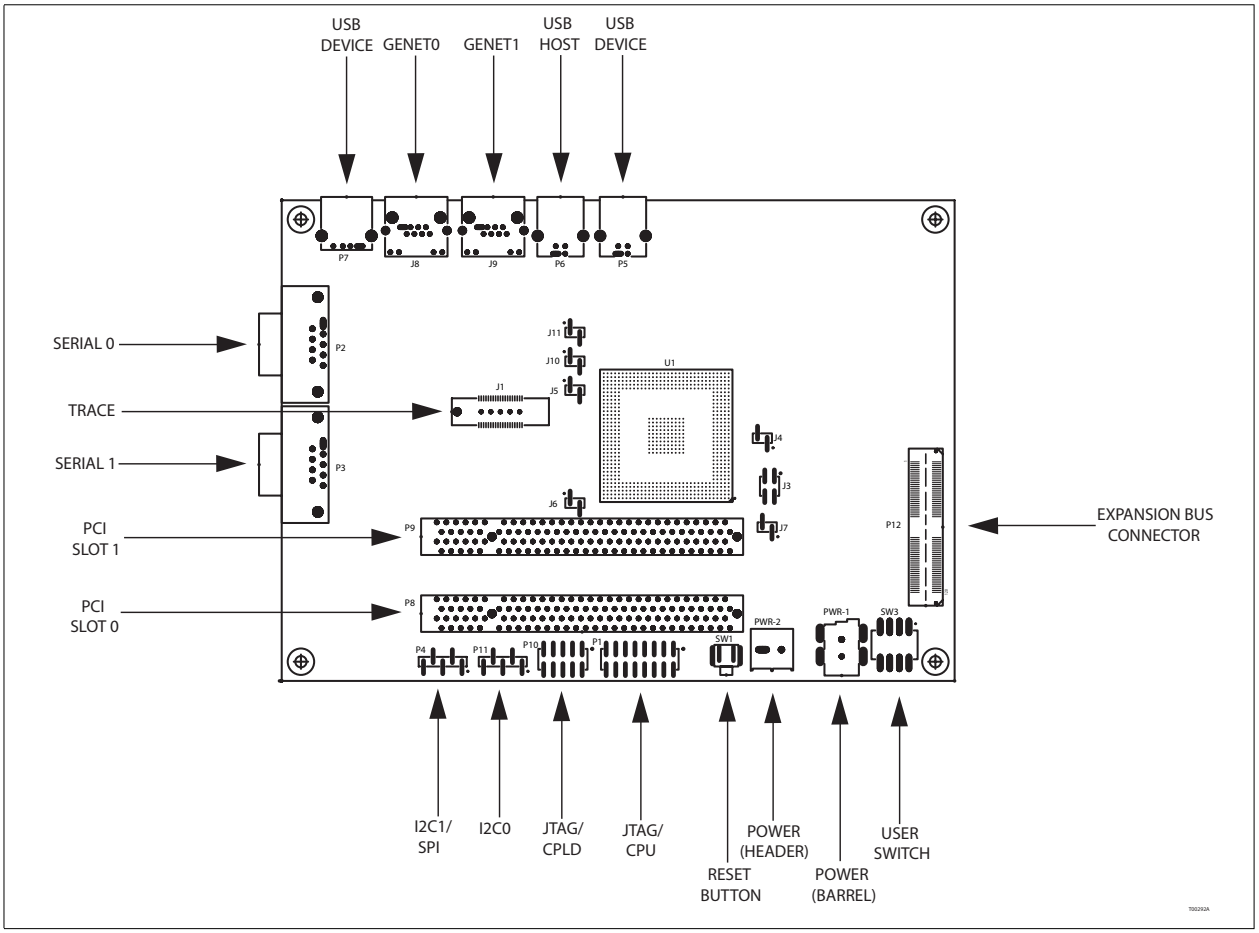

Figure 2-2. Evaluation Board - Front Connectors

input to the CPLD, a 48 MHz CPU USB 2.0 clock input and a 12 MHz clock input to the SMSC GT3200 USB 2.0 UTMI device.

Memory The board supports a single bank of 256 MByte DDR2 SDRAM. The memory features a 333 MHz data rate with a dedicated DDR2 interface and a x64 bus width. There is no ECC option. The memory includes (Table 1-1) DDR SDRAM (Micron/Infineon; refer to ***DDR2 SDRAM Organization*** in this chapter) and FLASH (Spansion: S29GLxxxX Mirror-Bit).

BCSR Board control and status registers (BCSR) provide hardware control and status to the processor. BCSR bits selectively enable/disable and configure board features, and control LEDs, read switch settings, and provide status indications. The BCSR registers of the evaluation board is implemented in control logic within a complex programmable logic device (CPLD). Refer to the Chapter 5 for BCSR programming information.

SEP There are three serial EEPROMs (SEPs) on the I2C bus: one standard and two boot sequencer. All three SEPs are 2-wire, Atmel 24C04 devices. SEP addresses are controlled by the CPLD. The standard SEP stores configuration parameters for the board including such things as the IP address, baud rate, etc.

The boot sequence SEP stores register information for the processor. One boot sequence SEP is for 33 MHz PCI operation and the other boot sequencer SEP is for

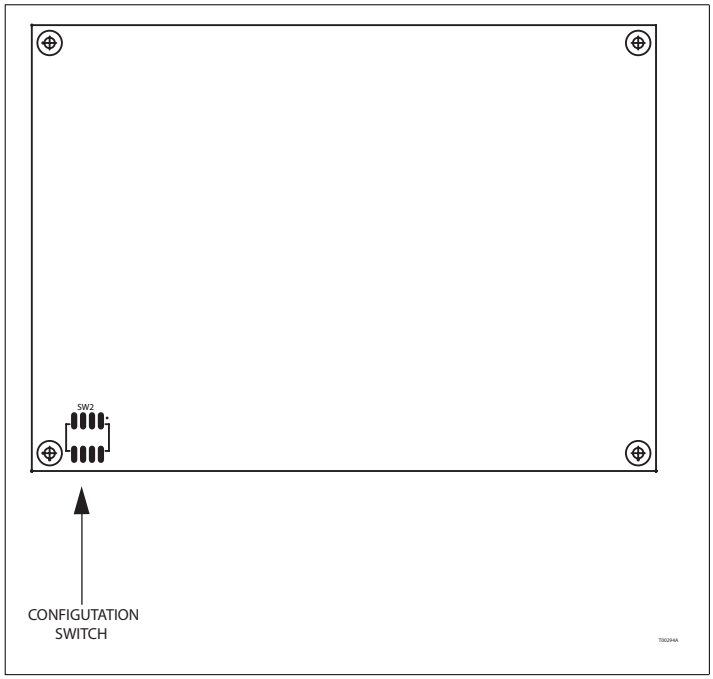

Figure 2-3. Evaluation Board - Back Connectors

66 MHz PCI operation. The boot sequencer SEP is enabled by BOOTSEQ bits of the reset configuration word. If enabled, the boot sequencer holds the processor core in reset until the boot sequence is complete. If disabled, the processor core exits reset and fetches boot code in default configurations. The boot sequencer SEP data must follow the format described in the processor user manual. Refer to the Chapter 7 for programming information for this I2C device.

The standard EEPROM (SEP) stores configuration parameters for the board. These configuration parameters are set using u-boot; refer to ***Firmware*** in this chapter. Refer to the Chapter 7 for programming information for this I2C device.

Table 2-1. SEP Addressing

Standard EEPROM Address (default)	0b1010100
Boot Sequence EEPROM Address	0b1010000

STTM

The serial temperature and thermal monitor (STTM) is an onboard temperature sensor. The STTM part is a 2-wire, digital temperature sensor. Its functionality is equivalent to the Analog Devices AD7414-0 part. The minimum resolution provided by this part is a 10-bit temperature conversion. Refer to the Chapter 7 for programming information for this I2C device.

Table 2-2. STTM Addressing

STTM_ADD Signal	Address
Float	0b1001 000 **(hard-coded default)**
GND	0b1001 001
VDD	0b1001 010

I/O

The evaluation board has:

- Two Gigabit Ethernet ports. These ports use a Marvell 88E1111 PHY using the AMCC 440RGMII interface. The fast Ethernet default PHY addresses are 0b00000 (ETH-0) and 0b00001 (ETH-1).
- Two DB-9 serial ports. The ports communicate via UART0 and UART1 of the processor. The serial ports use Intersil ICL3225E RS-232 transceivers or equivalent.
- Three USB ports. A USB 2.0 device uses a UTMI interface with a SMSC GT3200 transceiver or equivalent. A USB 2.0 host with a type A connector and a USB 2.0 device with a type B connector communicate directly with the PPC440EPx processor. USB is not available for the PPC440GRx processor.
- One JTAG/CPU port header for debugger use.
- One TRACE port header for debugger use.
- One JTAG/CPLD port header for CPLD programming only.
- One I2C1/SPI port header for user configuration.
- One I2C0 port header for user configuration.
- One GPIO port header for user configuration.

Refer to Chapter 3 for more information and pinouts for the connectors.

PCI

The processor's PCI interface is accessed via the two PCI slot connectors. The PPC440EPx or PPC440GRx processor provides a PCI arbiter.

NOTE: The evaluation board supports PCI host mode only.

Interrupt Control

Board and PCI interrupt requests are handled directly by the interrupt controller of the processor.

Performance Timer

The CPLD contains a 28 bit counter that is clocked at 33 MHz and is controlled by BCSR10. Refer to Chapter 5 for more information on the performance timer.

PowerPC Processor

The evaluation board incorporates an AMCC PowerPC 440EPx or PowerPC 440GRx embedded processor. This 32-bit reduced instruction set computer (RISC) processor includes an integrated PowerPC core and peripheral interfaces that can be used in a variety of controller applications. It is particularly well-suited for both communications and networking applications. The PPC440EPx or PPC440GRx provides high performance and low power consumption.

The processor has integrated peripheral functions for I/O interface, which include:

- On-chip Double Data Rate (DDR2) SDRAM controller.
- PCI interface.
- USB.
- FPU.
- External bus controller.
- Nand FLASH controller.
- DMA controller.

NOTE: FPU and USB are not supported by the PPC440GRx processor.

DDR2 SDRAM Organization

Memory Clock	166 MHz
Data Transfer Rate	333 MHz
256 MByte	512 Mbit (8M x 16 bit) devices 4 Micron MT47H32M16CC-3 16 MBytes x 4 banks x 4 devices = 256 MBytes total 2 bit bank address at 4(BA0, BA1) 13 bit row address at 8K (A0-A12) 10 bit column address at 1K (A0-A10)

FLASH Organization

This section summarizes the FLASH memory device currently used on the evaluation board. Refer to the Spansion MirrorBit and STMicro data sheets for detailed information about these FLASH memory devices. Figures 2-4 and 2-5 show the address and data line connections. An offset is needed when issuing commands to the FLASH device due to the address line connections. Tables 2-3 and 2-4 list the FLASH memory device IDs.

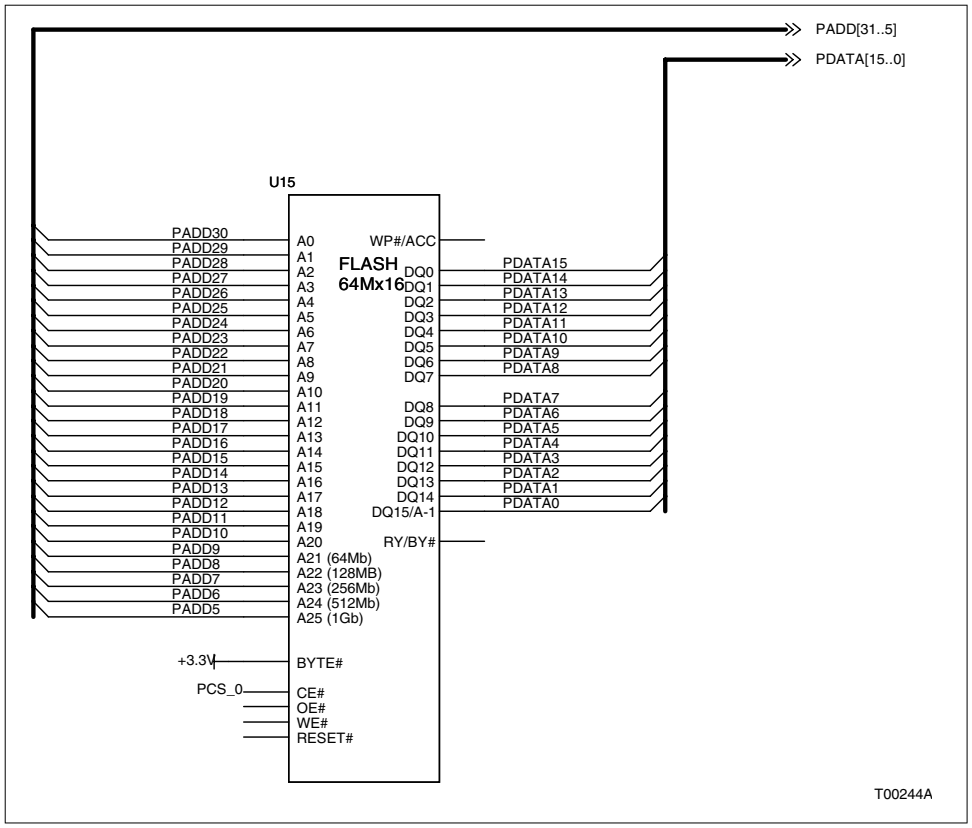

Figure 2-4. NOR FLASH Address and Data Lines

The following guidelines apply to x16 ported FLASH memory:

- FLASH device configured in 16-bit mode.

Table 2-3. NOR FLASH Device ID

Device	MFG ID	Device ID
S29GL256N	0x0001	0x2201

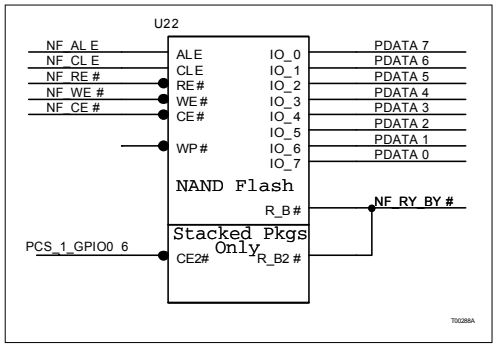

Figure 2-5. NAND FLASH Address and Data Lines

Table 2-4. NAND FLASH Device ID

Device	MFG ID	Device ID
K9F5608U0B	0xEC	0x75

- Sector and chip erases should be performed only on a long word basis.
- Programming should be done on a long word basis if possible.

I/O Interface Signals

Table 2-5 lists the I/O interface PowerPC 440 output signals used on the evaluation board.

Table 2-5. I/O Signals

Interface	Signal
System	$\overline{\text{SYSRESET}}$
	SYSCLK
	TMRCLK
	TESTEN
	SYSERR
	PSROOUT
Interrupts	IRQ0:9
Trace	TRCCLK
	TRCBS0:2
	TRCES0:4
	TRCTS0:6

Table 2-5. I/O Signals *(continued)*

Interface	Signal
JTAG	TCK
	TDO
	TDI
	TMS
	$\overline{\text{TRST}}$
External Slave Peripheral Interface	PERADDR2:31
	PERDATA0:15
	$\overline{\text{PERCS0:5}}$
	$\overline{\text{PEROE}}$
	$\overline{\text{PER\_W}}$
	$\overline{\text{PERWBE0:3}}$
	PERREADY
	$\overline{\text{PERBLAST}}$
External Master	$\overline{\text{EXTRESET}}$
	PERCLK
	PERERR
DDR SDRAM	MEMDATA0:63
	SVREF1A
	SVREF1B
	SVREF2A
	SVREF2B
	MEMADDR0:13
	BA0:3
	$\overline{\text{RAS}}$
	$\overline{\text{CAS}}$
	$\overline{\text{WE}}$
	DM0:8
	DQS0:8
	MEMODT0:1
	$\overline{\text{BANKSEL0:1}}$
	MEMCLKEN
	MEMCLKOUT
	$\overline{\text{MEMCLKOUT}}$

Table 2-5. I/O Signals *(continued)*

Interface	Signal
Serial ports	UART1_TX
	UART1_RX
	$\overline{\text{PERPAR1\_UART1\_RTS}}$
	$\overline{\text{PERPAR0\_UART1\_RTS}}$
	UART2_TX
	UART2_RX
	$\overline{\text{UART2\_RTS}}$
	$\overline{\text{UART2\_CTS}}$
	UARTSERCLK
I2C	I2C0SCLK
	I2C0SDATA
	SCPCLK
	SCPDI
	SCPDO
NAND FLASH Interface	NFALE
	NFCLE
	$\overline{\text{NFREN}}$
	$\overline{\text{NFWEN}}$
	$\overline{\text{NFRDYBUSY}}$
	$\overline{\text{NFCE3}}$
Gig-Ethernet RGMII0	GMC0_TXD0:3
	GMC0_TXCTL
	GMC0_TXCLK
	GMCTXCLK
	GMC0_RXD0:3
	GMC0_RXCTL
	GMC0_RXCLK
Gig-Ethernet RGMII1	GMC1_TXD0:3
	GMC1_TXCTL
	GMC1_TXCLK
	GMC1_RXD0:3
	GMC1_RXCTL
	GMC1_RXCLK
Ethernet Management	REJECTPKT0:1
	GMCMDCLK
	GMCMDIO
	GMCREFCLK

Table 2-5. I/O Signals *(continued)*

Interface	Signal
PCI Interface	PCIAD0:31
	$\overline{\text{PCIC0\_BE0:3}}$
	$\overline{\text{PCIFRAME}}$
	$\overline{\text{PCIDEVSEL}}$
	$\overline{\text{PCIIRDY}}$
	PCIPAR
	$\overline{\text{PCIPERR}}$
	$\overline{\text{PCIRESET}}$
	$\overline{\text{PCISERR}}$
	$\overline{\text{PCISTOP}}$
	$\overline{\text{PCITRDY}}$
	$\overline{\text{PCIREQ0:5}}$
	$\overline{\text{PCIGNT0:1}}$
	PCICLK
USB 2.0 Device	USB2DO0:7
	USB2DI0:7
	USB2TXVAL
	USB2RXACT
	$\overline{\text{EXTREQ}}$
	USB2XCVRSEL
	USB2TERMSEL
	USB2LS0:1
	USB2OM0:1
	USB2SUSP
USB 2.0 PHY Host / Device	USB2XCVR
	$\overline{\text{USB2XCVR}}$
	USB2REXT
	USB2XTAL
	$\overline{\text{USB2XTAL}}$

Firmware

U-boot is open source firmware for the embedded PowerPC architecture. It can be installed in a boot ROM and used to initialize and test hardware or to download and run application code.

The evaluation board is shipped with the u-boot firmware residing in FLASH memory. U-boot has a load address of 0xFFF8 0000. U-boot utilities provide the ability to initialize the CPU board and auto execute an operating system or appli-

cation. Refer to online u-boot documentation for complete information about u-boot boot loader and utilities.

NOTE: Caution should be taken when modifying FLASH sectors occupied by the u-boot boot loader. A debugger will need to be used to reprogram u-boot onto the target should u-boot become corrupted or erased.

Restoring MAC Addresses

The evaluation board can have up to four media access control (MAC) addresses assigned to it. The MAC address is the physical address of a device connected to a network, expressed as a 48-bit hexadecimal number. The boards are assigned MAC addresses during manufacture using the following convention:

Enet controller 1 MAC = 0x0010ECxxxxxx ORed with 0x000000000000
Enet controller 2 MAC = 0x0010ECxxxxxx ORed with 0x000000800000

where

xxxxxx	Evaluation board serial number. The serial number can be found in decimal form on a label affixed to the Ethernet port on the board (e.g., 007573).

For example, a board with a serial number of 007573 decimal (001D95 hexadecimal) has a MAC address of:

00:10:EC:00:1D:95 for Enet controller 1
00:10:EC:80:1D:95 for Enet controller 2

If it becomes necessary to restore a missing or corrupted MAC address, use the above convention to determine your evaluation board's MAC addresses and issue the following commands in u-boot:

setenv ethaddr *<MAC ADDRESS1>* **ENTER**

setenv eth1addr *<MAC ADDRESS2>* **ENTER**

saveenv ENTER

Connectors and Headers

Chapter 3

The evaluation board has the following connectors for I/O functions and expandability:

- Two RJ-45 connectors with integrated LEDs for fast Ethernet ports (10BaseT/100BaseTX/1000BaseT).
- Two DB-9 connectors for RS-232 serial ports.
- One barrel connector for power.
- One 1 x 2 header for power
- Three USB connectors.
- Two PCI slots.
- Six headers for auxiliary functions: JTAG/CPU, TRACE, JTAG/CPLD, I2C1/SPI, I2C0 and spare GPIO.

This chapter describes these connectors and headers. Refer to Figures 2-2 for the locations of these connectors and headers.

Power

There are two options for powering the evaluation board:

- +5 VDC supplied through the barrel connector.
- +5 VDC supplied through the 1 x 2 pin power header.

The +5 VDC barrel connector power option requires a regulated 4.75 to 5.25 VDC supply and supports up to 5 A (25 W). The evaluation board itself, fully configured, but with no PCI cards, draws 20 W maximum at VCC = 4.75 VDC to 5.25 VDC, T = 0° C to 70° C (32° F to 158° F). This leaves a total of 5 W between the 2 PCI cards when using the barrel connector.

The +5 VDC 1 x 2 power header power option requires a regulated 4.75 to 5.25 VDC supply and supports up to 16 A (80 W). The evaluation board itself, fully configured, but with no PCI cards, draws 20 W maximum at VCC = 4.75 VDC to 5.25 VDC, T = 0° C to 70° C (32° F to 158° F). This leaves a total of 60 W between the 2 PCI cards when using the 1 x 2 power header connector.

NOTES:

1. The PCI v2.2 specification limits a PCI expansion card to 25 W max.

2. The EP board's +3.3 VDC power supply can provide a total of 16 A with a maximum of 2.4 A required by the EP board. This leaves 13.6 A total for the two PCI expansion cards.

3. The 1 x 2 power header is fused with two parallel 10 A fuses which combined can accommodate a maximum of 16 A. Therefore, the user should ensure that the power supply in use is protected by these EP board fuses or provides its own over-current protection if it is unable to meet a 16 A demand.

Power Connectors

The power connector (PWR-1) is a barrel type connector. The specifications for the mating connector are as follows:

Inner diameter = 2.1 mm (0.083 inches)
Outer diameter = 6.5 mm (0.256 inches)
Barrel Length = 14.8 mm (0.583 inches)
Outer shell is GND
Inner shell is +5 VDC

The power connector (PWR-2) is a 1 x 2 pin header. This power connector can be used to provide custom power levels not achievable through the barrel connector. Table 3-1 shows the power connector pinout.

Table 3-1. Power Connector Pinout (PWR-2)

Pin	Function	Pin	Function
1	+5 VDC	2	GND

JTAG/CPU Port

The JTAG/CPU port is P1. It is a 2 x 8 (0.1 x 0.1) header. Table 3-2 shows the JTAG/CPU port pinout.

Table 3-2. JTAG/CPU Port Pinout (P1)

Pin	Function	Pin	Function
1	TDO	2	—
3	TDI	4	$\overline{\text{TRST}}$
5	—	6[1]	+3.3 VDC
7	TCK	8	—
9	TMS	10	—
11	$\overline{\text{HALT}}$	12	—
13	—	14	—
15	—	16	GND

NOTE:
1. Current limited with a 1K resistor.

TRACE Port

The TRACE port is J1. It is a Mictor connector. Table 3-3 shows the TRACE port pinout.

Table 3-3. TRACE Port Pinout (J1)

Pin	Function	Pin	Function
1	GND	2	GND
3	GND	4	GND
5	GND	6	TRC_CLK
7	$\overline{\text{HALT}}$	8	GND
9	GND	10	GND
11	TDO	12[1]	+3.3VDC
13	GND	14	GND
15	TCK	16	GND
17	TMS	18	GND
19	TDI	20	GND
21	$\overline{\text{TRST}}$	22	GND
23	GND	24	TRCES4
25	TRCBS0	26	TRCTS0
27	TRCBS1	28	TRCTS1
29	TRCBS2	30	TRCTS2
31	TRCES0	32	TRCTS3
33	TRCES1	34	TRCTS4
35	TRCES2	36	TRCTS5
37	TRCES3	38	TRCTS6

NOTE:
1. Current limited with a 1K resistor.

JTAG/CPLD Port

The JTAG/CPLD port is P10. It is a 2 x 5 (0.1 x 0.1) header. Table 3-4 shows the JTAG/CPLD port pinout.

Table 3-4. JTAG/CPLD Port Pinout (P10)

Pin	Function	Pin	Function
1	TCK	2	GND
3	TDO	4	+3.3 VDC
5	TMS	6	—
7	—	8	—
9	TDI	10	GND

Gigabit Ethernet Ports

The Gigabit Ethernet ports (10BaseT/100BaseTX/1000BaseT) are connectors J8 (RGMII0) and J9 (RGMII1). They are shielded RJ-45 jacks with integrated LEDs. Table 3-5 shows the RJ-45 jack pinout. The RJ-45 connectors are shielded and tied to GROUND.

Table 3-5. Fast Ethernet Port Pinout (J8, J9)

Pin	Function	Pin	Function
1	TXD+	5	—
2	TXD-	6	RXD-
3	RXD+	7	—
4	—	8	—

NOTE:
1. Pin numbering is from right (1) to left (8) when looking into the RJ-45 jack with the locking tab on top.

Serial Ports

Serial port 0 (UART0) is P2 and serial port 1 (UART1) is P3. They are DB-9 Molex 87204-6043 headers. The serial ports are wired as DTE. Table 3-6 shows the serial port pinout.

Table 3-6. Serial Port Pinout (P2, P3)

Pin	Function	Pin	Function
1	—	2	UART_RX
3	UART_TX	4	+5V
5	—	6	—
7	$\overline{\text{UART\_RTS}}$	8	$\overline{\text{UART\_CTS}}$
9	—	—	—

USB Ports

Only the PPC440EPx processor supports USB. The PPC440GRx processor does not support USB. The USB ports are P5 (USB 2.0 device), P6 (USB 2.0 device) and P7 (USB 2.0 host). P5 and P6 use a USB type B connector and P7 uses a USB type A connector. Table 3-7 shows the USB port pinout. All connectors are tied to ground.

Table 3-7. USB Port Pinout (P5, P6, P7)

Pin	Function	Pin	Function
1	USB_VCC	3	USB D+
2	USB D-	4	GND

I2C0 Port

The I2C0 port is P11. It is a 1 x 5 (0.1 x 0.1) header. This header allows access to the I2C0 signals. Table 3-8 shows the I2C0 port pinout.

Table 3-8. I2C0 Port Pinout (P11)

Pin	Function
1	I2C0_SCLK
2	+3.3VDC
3	I2C0_SDATA
4	GND
5	—

I2C1/SPI Port

The I2C1/SPI port is P4. It is a 1 x 5 (0.1 x 0.1) header. This header allows port 1 of the I2C bus to be configured as a second I2C or SPI port. Table 3-9 shows the I2C1/SPI port pinout.

Table 3-9. I2C1/SPI Port Pinout (P4)

Pin	Function
1	SCPClkOut_I2C1SClk
2	+3.3 VDC
3	SCPDI_I2C1SData
4	GND
5	SCPDO

Jumpers

There are 5 jumper pairs that allow for a variety of signal testing. Table 3-10 shows the signals for these jumpers.

Table 3-10. Jumpers (J2, J3, J4, J5, J6, J7)

Jumper	Pin	Signal	Pin	Signal
J2	1	GND	2	BOOT_NOR
J3	1	+1.5 VDC_CPU	2	+1.5 VDC
J3	3	+1.5 VDC_CPU	4	+1.5 VDC
J4	1	+1.8 VDC	2	+1.8 VDC_CPU
J5	1	+2.5 VDC	2	+2.5 VDC_CPU
J6	1	+3.3 VDC	2	+3.3 VDC_CPU
J7	1	GND	2	PerClk

Expansion Bus Connector

The expansion bus connector is P12. It is a 2 x 60 (B8 Type) receptacle. This interface allows daughter cards to be designed and interfaced to the EP board.

Important The expansion bus connector must be a +3.3 VDC only type of interface (the I/O is not +5 VDC I/O tolerant).

NOTES:

1. External mastering is not supported.

2. The expansion bus connector is not installed in the default board configuration. If an installed expansion bus connector is required, a custom assembly should be obtained by contacting sequoiasupport@amcc.com or rainiersupport@amcc.com.

Table 3-11. Expansion Bus Connector (P12)

Pin	Signal	Signal	Pin
1	PADD31	PDATA31	2
3	PADD30	PDATA30	4
5	PADD29	PDATA29	6
7	PADD28	PDATA28	8
9	PADD27	PDATA27	10
11	PADD26	PDATA26	12
13	PADD25	PDATA25	14
15	PADD24	PDATA24	16
17	PADD23	PDATA23	18
19	PADD22	PDATA22	20
21	PADD21	PDATA21	22
23	PADD20	PDATA20	24
25	PADD19	PDATA19	26
27	PADD18	PDATA18	28
29	PADD17	PDATA17	30
31	PADD19	PDATA16	32
33	PADD15	PDATA15	34
35	PADD14	PDATA14	36
37	PADD13	PDATA13	38
39	PADD12	PDATA12	40
41	PADD11	PDATA11	42
43	PADD10	PDATA10	44
45	PADD9	PDATA9	46
47	PADD8	PDATA8	48
49	PADD7	PDATA7	50
51	PADD6	PDATA6	52
53	PADD5	PDATA5	54
55	PADD4_GPIO3	PDATA4	56
57	PADD3_GPIO2	PDATA3	58
59	PADD2_GPIO1	PDATA2	60
61	PCS_1_GPIO06	PDATA1	62
63	PCS_1_GPIO09	PDATA0	64
65	PCS_1_GPIO010	—	66

Table 3-11. Expansion Bus Connector (P12) *(continued)*

Pin	Signal	Signal	Pin
67	$\overline{\text{POE}}$	GPIO27	68
69	PR_$\overline{\text{W}}$	GPIO28	70
71	PWBE_$\overline{0}$	PERPAR0_UART1_$\overline{\text{CTS}}$	72
73	PWBE_$\overline{1}$	PERPAR0_UART1_$\overline{\text{RTS}}$	74
75	PWBE_$\overline{2}$	PERPAR0_GPIO32	76
77	PWBE_$\overline{3}$	PERPAR0_GPIO33	78
79	PREADY	GPIO44	80
81	$\overline{\text{PBLAST}}$	GPIO45	82
83	EXT_$\overline{\text{RESET}}$	GPIO46	84
85	CLK_PERCLK	GPIO47	86
87	PERERR_GPIO11	GPIO48	88
89	—	—	90
91	—	—	92
93	—	—	94
95	—	—	96
97	—	—	98
99	—	—	100
101	—	—	102
103	—	—	104
105	—	SPARE_0	106
107	—	SPARE_1	108
109	I2C0_SCLK	SPARE_2	110
111	I2C0_SDATA	SPARE_3	112
113	GNDSCPCLK	SPARE_4	114
115	SCPDI	SPARE_5	116
117	SCPDO	SPARE_6	118
119	$\overline{\text{RESET\_CPLD}}$	SPARE_7	120

PCI Edge Slots

The PCI edge slots are P8 and P9. They are standard 4 x 30, 2 millimeter connectors as defined by the +3.3 VDC, 32-bit, 62-pin, PCI edge specification. This interface allows PCI add-on boards to be interfaced to the evaluation board.

Table 3-12. PCI Edge Connector (P8, P9)

Pin	Signal	Signal	Pin
B1	-12 VDC	GND	A1
B2	GND	+12 VDC	A2
B3	GND	+3.3 VDC	A3
B4	—	+3.3 VDC	A4

Table 3-12. PCI Edge Connector (P8, P9) *(continued)*

Pin	Signal	Signal	Pin
B5	+5 VDC	+5 VDC	A5
B6	+5 VDC	$\overline{\text{PCI\_INTA}}$	A6
B7	$\overline{\text{PCI\_INTA}}$	$\overline{\text{PCI\_INTA}}$	A7
B8	$\overline{\text{PCI\_INTA}}$	+5VDC	A8
B9	GND	—	A9
B10	—	+3.3 VDC	A10
B11	GND	—	A11
B12	— [KEY]	— [KEY]	A12
B13	— [KEY]	— [KEY]	A13
B14	—	+3.3 VDC	A14
B15	GND	$\overline{\text{PCI\_RST}}$	A15
B16	CLK_PCI2_66/33	+3.3 VDC	A16
B17	GND	$\overline{\text{PCI\_GNTN}}$	A17
B18	$\overline{\text{PCI\_REQN}}$	GND	A18
B19	+3.3 VDC	—	A19
B20	PCI_AD31	PCI_AD30	A20
B21	PCI_AD29	+3.3 VDC	A21
B22	GND	PCI_AD28	A22
B23	PCI_AD27	PCI_AD26	A23
B24	PCI_AD25	GND	A24
B25	+3.3 VDC	PCI_AD24	A25
B26	$\overline{\text{PCI\_C/BE3}}$	PCI_IDSEL	A26
B27	PCI_AD23	+3.3 VDC	A27
B28	GND	PCI_AD22	A28
B29	PCI_AD21	PCI_AD20	A29
B30	PCI_AD19	GND	A30
B31	+3.3 VDC	PCI_AD18	A31
B32	PCI_AD17	PCI_AD16	A32
B33	$\overline{\text{PCI\_C/BE2}}$	+3.3 VDC	A33
B34	GND	$\overline{\text{PCI\_FRAME}}$	A34
B35	$\overline{\text{PCI\_IRDY}}$	GND	A35
B36	+3.3 VDC	$\overline{\text{PCI\_TRDY}}$	A36
B37	$\overline{\text{PCI\_DEVSEL}}$	GND	A37
B38	GND	$\overline{\text{PCI\_STOP}}$	A38
B39	$\overline{\text{PCI\_LOCK}}$	+3.3 VDC	A39
B40	$\overline{\text{PCI\_PERR}}$	+3.3 VDC	A40
B41	+3.3 VDC	+3.3 VDC	A41
B42	$\overline{\text{PCI\_SERR}}$	GND	A42
B43	+3.3 VDC	PCI_PAR	A43
B44	$\overline{\text{PCI\_C/BE1}}$	PCI_AD15	A44
B45	PCI_AD14	+3.3 VDC	A45

Table 3-12. PCI Edge Connector (P8, P9) *(continued)*

Pin	Signal	Signal	Pin
B46	GND	PCI_AD13	A46
B47	PCI_AD12	PCI_AD11	A47
B48	PCI_AD10	GND	A48
B49	M66EN	PCI_AD09	A49
B50	GND	GND	A50
B51	GND	GND	A51
B52	PCI_AD08	$\overline{\text{PCI\_C/BE0}}$	A52
B53	PCI_AD07	+3.3 VDC	A53
B54	+3.3 VDC	PCI_AD06	A54
B55	PCI_AD05	PCI_AD04	A55
B56	PCI_AD03	GND	A56
B57	GND	PCI_AD02	A57
B58	PCI_AD01	PCI_AD00	A58
B59	+3.3 VDC	+3.3 VDC	A59
B60	$\overline{\text{PCI\_ACK64}}$	$\overline{\text{PCI\_REQ64}}$	A60
B61	+5VDC	+5VDC	A61
B62	+5VDC	+5VDC	A62

Operation

Chapter 4

This chapter describes the LED indications for the evaluation board. It also provides some switch, u-boot description and communication information.

Board LEDs

The CR1, CR2 and CR3 LEDs signal the applied voltages to the board.The two user-programmable LEDs (Table 4-1) are under BCSR control. The SYSERR signal is used to drive the status LED and is active when high. Refer to Table 5-3 for LED control bit information. Refer to Figure 2-2 for the locations of the LEDs.

Table 4-1. Board LED Definition

LED	Signal	Color
CR1	+5 VDC	Green
CR2	+3.3 VDC	Green
CR3	USER_LED0	Green
CR4	USER_LED1	Green
CR5	$\overline{\text{SYSERR}}$	Red
CR6	$\overline{\text{RESET\_BUFPOR}}$	Red

Fast Ethernet Port LEDs

Table 4-2 describes the indications given by the fast Ethernet ports LEDs (J8 and J9); refer to Figure 2-2 for the location of these ports. These LEDs are integrated into the Ethernet port.

Table 4-2. Fast Ethernet Port LEDs

State	Indication	
	Left LED (LED2)	Right LED (LED1)
Off	Link integrity valid and is using 10 Mbps Ethernet Flashes with RXD and TXD activity	—
Yellow	Link integrity valid and is using 100 Mbps Ethernet Flashes with RXD and TXD activity	Half-duplex Ethernet
Green	Link integrity valid and is using 1000 Mbps Ethernet Flashes with RXD and TXD activity	Full-duplex Ethernet

Switches

Configuration Switch

The four pole boot configuration switch (SW2) is used for the bootstrap selection.

NOTE: SW2 is factory set. This switch should **not** be changed unless it is desired to change the board to boot-from-NAND FLASH instead of its default boot-from-NOR FLASH. The NAND FLASH will need to be programmed prior to changing the boot option. Refer to ***NAND FLASH Programming*** for the steps to program the NAND FLASH.

Table 4-3. Boot Configuration Switch (SW2) Settings

Purpose	Pole Position SW2: 4 3 2 1 D(3:0)	Function
Boot using I2C Bootstrap Controller[1]	x111	I2C bootstrap controller enabled; bootstrap option H (refer to PPC440EPx or PPC440GRx User Manual).
For testing purposes only	1xxx	Normal operation

NOTES:
on = closed position will read back a logic 0 in the status register.
off = open position will read back a logic 1 in the status register.
1. Jumper J2 should not be populated for boot-from-NOR; jumper J2 should be populated for boot-from-NAND. refer to ***FLASH Boot Select*** in this chapter.

User Switch

The four-pole user switch (SW3) located on the board is readable via the onboard status register (Table 5-3). The switch is intended for user applications.

Memory Map

Table 4-4 describes the memory map for the evaluation board.

Table 4-4. Memory Map

Function	Start Address	End Address	Size	Chip Select
DDR SDRAM	0x0000 0000	0x0FFF FFFF	256 MB	—
PCI Memory	0x8000 0000	0xBFFF FFFF	1024 MB	—
BCSR	0xC000 0000	0xCFFF FFFF	256 MB	$\overline{CS2}$
NAND FLASH Controller[1]	0xD000 0000	0xD00F FFFF	1 MB	$\overline{CS3}$/$\overline{CS0}$
NOR FLASH[1]	0xFC00 0000	0xFFFF FFFF	64 MB	$\overline{CS0}$/$\overline{CS3}$

NOTE:
1. NOR FLASH and NAND FLASH chip selects depend on jumper J2 settings; refer to FLASH Boot Select for details.

NAND Boot Configuration

Three different setup steps are required to change the board from its default boot-from-NOR FLASH configuration to a boot-from-NAND FLASH configuration.

1. The NAND FLASH must be programmed with a u-boot image that supports boot-from-NAND FLASH operation; refer to ***NAND FLASH Programming*** in this chapter.

2. The boot EEPROMs must be reprogrammed for boot-from-NAND FLASH operation; refer to ***Restoring the Boot EEPROM*** in Chapter 7.

3. The boot select jumper needs to be set appropriately; refer to ***FLASH Boot Select*** in this chapter.

NAND FLASH Programming

The default configuration for the evaluation board is to have a non-programmed NAND FLASH device. The following procedure must be followed in order to have a bootable NAND FLASH device:

1. Load the NAND FLASH u-boot image over TFTP onto the evaluation board.

NOTE: The NAND FLASH u-boot image must reside in a location on the host that is accessible by a working TFTP server.

=> **tftp 100000 u-boot-nand.bin ENTER**

2. Erase the NAND FLASH device.

=> **nand erase 0 60000 ENTER**

3. Load the NAND FLASH u-boot image into FLASH.

=> **nand write 100000 0 60000 ENTER**

The NAND FLASH u-boot image should now reside in the NAND FLASH device. In order to boot from the NAND FLASH device; refer to the ***FLASH Boot Select*** section in this chapter.

FLASH Boot Select

The processor can be configured to boot from the NOR FLASH or the NAND FLASH. To accommodate this, a set of muxes were added to connect the processors $\overline{CS0}$ and $\overline{CS3}$ to the NOR FLASH or NAND FLASH as determined by jumper, J2.

Boot-from-NOR

To boot from the NOR FLASH, jumper J2 should not be populated. The boot EEPROM should be programmed with boot-from-NOR configuration; refer to Table 4-3.

Boot-from-NAND

To boot from the NAND FLASH, the jumper J2 should be populated. The boot EEPROM should be programmed with boot-from-NAND configuration; refer to Table 4-3.

NOTE: Before configuring the NAND FLASH boot settings, the NAND FLASH device must be programmed; refer to ***NAND FLASH Programming*** in this chapter.

Table 4-5. FLASH Boot Select

Jumper (J2)	Boot FLASH	NOR FLASH Chip Select	NAND FLASH Chip Select
Off	NOR FLASH	$\overline{CS0}$ ($\overline{PCS0}$)	$\overline{CS3}$ ($\overline{NF\_CE}$)
On	NAND FLASH	$\overline{CS3}$ ($\overline{NF\_CE}$)	$\overline{CS0}$ ($\overline{PCS0}$)

RS-232 Connection

A DB-9 is required for RS-232 communication. Table 3-6 provides the pinout for the header. The evaluation board has its serial ports wired as DTE. A null modem is required when interfacing to a DTE port.

For DTE:

DB9-3 = TXD
DB9-2 = RXD
DB9-8 = $\overline{\text{CTS}}$
DB9-7 = $\overline{\text{RTS}}$
DB9-5 = GND

User Applications

U-boot assumes the board is connected to a dumb terminal or a PC-based terminal emulator, and requires user intervention for the diagnostics. The dumb terminal or PC serial port should be set as follows:

- 115200 baud (default).
- 8 data bits.
- 1 stop bit.
- No parity.
- No hardware handshake.

Proper interfacing to the serial port via the correct RS-232 connections must be insured as described in ***RS-232 Connection*** in this chapter. The dumb terminal or PC serial port might require the $\overline{\text{CTS}}$ signal to be true. In this case, the $\overline{\text{RTS}}$ signal, which is driven from the serial port, should also be connected in the cable path to the $\overline{\text{CTS}}$ signal on the dumb terminal or PC serial port.

Board Control and Status Registers

Chapter 5

The evaluation board has onboard control and status registers. These registers are configured as x8 ports. The registers are defined as shown in Tables 5-1 through 5-14. Refer to ***Memory Map*** in Chapter 4 for the default base memory address for accessing the BCSR registers.

NOTES:

1. Bit 0 is the MSB and bit 7 is the LSB.

2. The value of X in reset values is determined by the value of a CPLD input during Power-On-Reset.

Register values at reset (values in binary):

Register 0 = ID	Board ID
Register 1 = 0000 0000	CPLD revision
Register 2 = 0000 xxxx	User switch / LEDs
Register 3 = 0000 xxxx	Configuration switch
Register 4 = 0000 0000	TMRCLK control
Register 5 = 0000 0000	PCI control, status, info
Register 6 = 0000 0000	Reset control
Register 7 = 0000 001x	Memory control
Register 8 = 0000 0000	Ethernet control
Register 9 = 0000 0001	USB control
Register 10 = 0000 0000	Performance timer (MS Byte, bits 27-24)
Register 11 = 0000 0000	Performance timer (bits 23-16)
Register 12 = 0000 0000	Performance timer (bits 15-8)
Register 13 = 0000 0000	Performance timer (LS Byte, bits 7-0)

Table 5-1. BCSR0 - Board ID

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x0 reset value = ID	ID	0	RO	ID = 0000 1111 = EP440xC 1.1
		1	RO	
		2	RO	
		3	RO	
		4	RO	
		5	RO	
		6	RO	
		7	RO	

Table 5-2. BCSR1 - CPLD revision

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x1 reset value = REV	CPLD REV	0	RO	REV = revision of CPLD code
		1	RO	
		2	RO	
		3	RO	
		4	R0	
		5	RO	
		6	RO	
		7	RO	

Table 5-3. BCSR2 - User Switch / LEDs

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x2 reset value = 1100 xxxx	USER_LED0	0	R/W	0 = LED on 1 = LED off
	USER_LED1	1	R/W	
	Reserved	2	RO	
		3	RO	
	User switch	4	RO	Switch closed = logic 0 = on Switch open = logic 1 = off Bit 4 = switch 4, bit 5 = switch 3, bit 6 = switch 2, bit 7 = switch 1
		5	RO	
		6	RO	
		7	RO	

Table 5-4. BCSR3 - Configuration Switch

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x3 reset value = 0000 0xxx	SysClk input	0	RO	0 = 33.0MHz 1 = 33.333MHz
	Reserved	1	RO	
		2	RO	
		3	RO	
		4	RO	
	Configuration switch	5	RO	Switch closed = logic 0 = on Switch open = logic 1 = off Bit 5 = switch 3, bit 6 = switch 2, bit 7 = switch 1
		6	RO	
		7	RO	

Table 5-5. BCSR4 - TMRCLK control

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x4 reset value = 0000 0000	Reserved	0	RO	
		1	RO	
		2	RO	
	TMRCLK source select	3	R/W	0 = 50 MHz 1 = PERCLK
	TMRCLK modifier	4	R/W	TMRCLK divider 0 = divide source by 1 Otherwise = divide source by 2x this value
		5	R/W	
		6	R/W	
		7	R/W	

Table 5-6. BCSR5 - PCI control, status, info

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x5 reset value = x000 0000	M66EN[1]	0	RO	0 = PCI operating at 33 MHz 1 = PCI operating at 66 MHz
	Reserved	1	RO	
		2	RO	
		3	RO	
		4	RO	
		5	RO	
		6	RO	
		7	RO	

Table 5-7. BCSR6 - Reset Control

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x6 reset value = 0000 0000	Reserved	0	RO	
		1	RO	
		2	RO	
		3	RO	
	Enable resets	4	R/W	0 = board resets disabled 1 = board resets enabled
	Reserved	5	RO	
		6	RO	
	POREST	7	R/W	0 = board reset not asserted 1 = board reset asserted

Table 5-8. BCSR7 - Memory control

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x7 reset value = x100 0000	FLASH	0	RO	0 = FLASH operation executing and busy 1 = FLASH operation complete (ready)
		1	R/W	0 = FLASH boot sector ***not*** write protected 1 = FLASH boot sector write protected
	EEPROM	2	R/W	0 = user EEPROM ***not*** write protected 1 = user EEPROM write protected
		3	R/W	0 = boot EEPROM ***not*** write protected 1 = boot EEPROM write protected
	NAND FLASH	4	R/W	0 = NAND FLASH ***not*** write protected 1 = NAND FLASH write protected
	Reserved	5	RO	
		6	RO	
		7	RO	

Table 5-9. BCSR8 - Ethernet control

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x8 reset value = 1010 0000	Ethernet PHY 0	0	R/W	1 = Assert 10/100/1000 Ethernet PHY 0 reset
		1	R/W	1 = Power down 10/100/1000 Ethernet PHY 0
	Ethernet PHY 1	2	R/W	1 = Assert 10/100/1000 Ethernet PHY 1 reset
		3	R/W	1 = Power down 10/100/1000 Ethernet PHY 1
	Reserved	4	RO	
		5	RO	
		6	RO	
		7	RO	

Table 5-10. BCSR9 - USB control

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0x9 reset value = 1x10 0x00	USB 2.0	0	R/W	USB2_RESET 0 = reset asserted 1 = de-assert reset; will be synchronized with rising edge of CLK_USB2
		1	RO	USB_2_VCC_PE for External PHY, 1 = device cable present
		2	R/W	USB / EBC# Mux Select 0 = peripheral bus shared IOs to connector 1 = route USB shared IOs to external PHY
	Reserved	3	RO	
		4	RO	
	USB 2.0	5	RO	USB_2_VCC_PI for Internal PHY, 1 = device cable present
	Reserved	6	RO	
		7	RO	

Table 5-11. BCSR10 - Performance timer (MS Byte, bits 27-24)

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0xA reset value = 0000 0000	Start, Stop	0	R/W	0 = stop 1 = start
	Latch count	1	R/W	1 = count latched to registers, counter remains counting This bit will always read 0
	Reserved	2	RO	
	Clear	3	R/W	1 = clear This bit will always read 0 Writing a 1 will clear all count registers to 0x000
	Counter	4	RO	Most significant Byte, bits 27-24
		5	RO	
		6	RO	
		7	RO	

Table 5-12. BCSR11 - Performance timer (bits 23-16)

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0xB reset value = 0000 0000	Counter	0	RO	Bits 23-16
		1	RO	
		2	RO	
		3	RO	
		4	RO	
		5	RO	
		6	RO	
		7	RO	

Table 5-13. BCSR12 - Performance timer (bits 15-8)

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0xC reset value = 0000 0000	Counter	0	RO	Bits 15-8
		1	RO	
		2	RO	
		3	RO	
		4	RO	
		5	RO	
		6	RO	
		7	RO	

Table 5-14. BCSR13 - Performance timer (LS Byte, bits 7-0)

Byte Address	Function	Bit	R/W	Definition
Base Addr + 0xD reset value = 0000 0000	Counter	0	RO	Bits 7-0
		1	RO	
		2	RO	
		3	RO	
		4	RO	
		5	RO	
		6	RO	
		7	RO	

Parametric Information

Chapter 6

The following section defines the hardware specific register and memory settings required for proper operation of the evaluation board.

FLASH (CS0)

Table 6-1. Peripheral Bank 0 Access Parameters - (Offset 0x0010)

Initial	Bit	Field	Value	Description
0x03017300	0	BME	0	Burst mode enable.
	1:8	TWT	00000110	Transfer wait (6 PerClk cycles).
	9:11	—	000	Reserved.
	12:13	CSN	00	Chip select on timing (0 PerClk cycles).
	14:15	OEN	01	Output enable on timing (1 PerClk cycles).
	16:17	WBN	01	Write Byte enable on timing (1 PerClk cycles).
	18:19	WBF	11	Write Byte enable off timing (3 PerClk cycles).
	20:22	TH	001	Transfer hold (1 PerClk cycles).
	23	RE	1	Ready enable.
	24	SOR	0	Sample on ready (data transfer occurs one PerClk cycle after PerReady is sampled active).
	25	BEM	0	Byte enable mode (PerWBE0:1 are only active for write cycles).
	26	PEN	0	Disable Parity checking for this bus region.
	27:31	—	00000	Reserved.

Table 6-2. Peripheral Bank 0 Configuration Register - (Offset 0x0000)

Initial	Bit	Field	Value	Description
0xFC0DA000	0:11	BAS	111111100 000	Base address select. 64 Meg, 16 bit at 0xFC000000.
	12:14	BS	110	Bank size (64 MB bank).
	15:16	BU	11	Bank usage (read/write).
	17:18	BW	01	Bus width (16-bit bus).
	19:31	—	000000000 0000	Reserved.

CPLD (CS2)

Table 6-3. Peripheral Bank 5 Access Parameters - (Offset 0x0012)

Initial	Bit	Field	Value	Description
0x24814580	0	BME	0	Burst mode enable.
	1:8	TWT	01001001	Transfer wait (73 PerClk cycles).
	9:11	—	000	Reserved.
	12:13	CSN	00	Chip select on timing (0 PerClk cycles).
	14:15	OEN	01	Output enable on timing (1 PerClk cycles).
	16:17	WBN	01	Write Byte enable on timing (1 PerClk cycles).
	18:19	WBF	00	Write Byte enable off timing (0 PerClk cycles).
	20:22	TH	010	Transfer hold (2 PerClk cycles).
	23	RE	1	Ready enable.
	24	SOR	1	Sample on ready (data transfer occurs in the same PerClk cycle that PerReady becomes active).
	25	BEM	0	Byte enable mode (PerWBE0:1 are only active for write cycles).
	26	PEN	0	Disable Parity checking for this bus region.
	27:31	—	00000	Reserved.

Table 6-4. Peripheral Bank 5 Configuration Register - (Offset 0x0002)

Initial	Bit	Field	Value	Description
0xC0038000	0:11	BAS	110000000 000	Base address select. 2 Meg, 16 bit at 0xC0000000.
	12:14	BS	001	Bank size (2 MB bank).
	15:16	BU	11	Bank usage (read/write).
	17:18	BW	00	Bus width (16-bit bus).
	19:31	—	000000000 0000	Reserved.

NAND FLASH (CS3)

Table 6-5. Peripheral Bank 5 Access Parameters - (Offset 0x0013)

Initial	Bit	Field	Value	Description
0x7F8FFE80	0	BME	0	Burst mode enable.
	1:8	TWT	11111111	Transfer wait (255 PerClk cycles).
	9:11	—	000	Reserved.
	12:13	CSN	11	Chip select on timing (3 PerClk cycles).
	14:15	OEN	11	Output enable on timing (3 PerClk cycles).
	16:17	WBN	11	Write Byte enable on timing (3 PerClk cycles).
	18:19	WBF	11	Write Byte enable off timing (3 PerClk cycles).
	20:22	TH	111	Transfer hold (7 PerClk cycles).
	23	RE	0	Ready enable.
	24	SOR	1	Sample on ready (data transfer occurs in the same PerClk cycle that PerReady becomes active).
	25	BEM	0	Byte enable mode (PerWBE0:1 are only active for write cycles).
	26	PEN	0	Disable Parity checking for this bus region.
	27:31	—	00000	Reserved.

Table 6-6. Peripheral Bank 5 Configuration Register - (Offset 0x0003)

Initial	Bit	Field	Value	Description
0xD00FC000	0:11	BAS	100000000 000	Base address select. 1 Meg, 16 bit at 0xD0000000.
	12:14	BS	111	Bank size (128 MB bank).
	15:16	BU	11	Bank usage (read/write).
	17:18	BW	10	Bus width (32-bit bus).
	19:31	—	000000000 0000	Reserved.

SDRAM Controller (DDR SDRAM)

Table 6-7. DDR0_02 - (Offset 0x0002)

Initial	Bit	Field	Value	Description
0x0000000	31:26	—	000000	Reserved.
	25:24	MAXCS	00	Maximum number of chip selects available
	23:20	—	0000	Reserved.
	19:16	MAXCOL	0000	Maximum width of column address in DRAMs
	15:12	—	0000	Reserved.
	11:8	MAXROW	0000	Maximum width of memory address bus (0 row bits)
	7:1	—	0000000	Reserved.
	0	START	0	Controller is not in active mode

Table 6-8. DDR0_00 - (Offset 0x0000)

Initial	Bit	Field	Value	Description
0x0000190A	31	—	0	Reserved.
	24:30	INTACK	0000000	Clear mask of the INT_STATUS parameter.
	16:23	INTSTA	00000000	Status of the interrupts in the controller.
	15	—	0	Reserved.
	8:14	DLLINC	0011001	Number of elements to add to DLL_START_POINT when searching for lock.
	7	—	0	Reserved.
	0:6	DLLSP	0001010	Initial delay count when searching for lock in master DLL.

Table 6-9. DDR0_01 - (Offset 0x0001)

Initial	Bit	Field	Value	Description
0x01000000	31:29	—	0	Reserved.
	28:24	CSLO	0000001	PLB DATABAHN CS lower address.
	23:21	—	000	Reserved.
	20:16	CSUP	00000	PLB DATABAHN CS upper address.
	15:11	—	00000	Reserved.
	10:8	OORTYP	000	Type of command that caused an Out-of-Range interrupt.
	7:0	INTMSK	00000000	Mask for controller interrupt signals from the INT_STATUS parameter.

Table 6-10. DDR0_03 - (Offset 0x0003)

Initial	Bit	Field	Value	Description
0x02030602	31:27	—	00000	Reserved.
	26:24	BSTLEN	010	Encoded burst length sent to DRAMs during initialization (4 words).
	23:19	—	00000	Reserved.
	18:16	CAS	011	Encoded CAS latency sent to DRAMs during initialization
	15:12	—	0000	Reserved.
	11:8	CLATLN	0110	Sets latency from read command send to data receive from/to controller (3 cycles).
	7:4	—	0000	Reserved.
	3:0	INAREF	0010	Number of auto-refresh commands to execute during DRAM initialization.

Table 6-11. DDR0_04 - (Offset 0x0004)

Initial	Bit	Field	Value	Description
0x13030300	31:29	—	000	Reserved.
	28:24	TRC	10011	Maximum number of chip selects available
	23:19	—	0000	Reserved.
	18:16	TRRD	011	Maximum width of column address in DRAMs
	15:11	—	00000	Reserved.
	10:8	TRTP	011	Maximum width of memory address bus (0 row bits)
	7:0	—	00000000	Reserved.

Table 6-12. DDR0_05 - (Offset 0x0005)

Initial	Bit	Field	Value	Description
0x0202050E	31:29	—	000	Reserved.
	28:24	TMRD	00010	DRAM TMRD parameter in cycles.
	23:19	—	0000	Reserved.
	18:16	TEMRS	010	DRAM TEMRS parameter in cycles.
	15:12	—	00000	Reserved.
	11:8	TRP	0101	DRAM TRP parameter in cycles.
	7:0	TRASMN	00001110	DRAM TRAS_MIN parameter in cycles.

Table 6-13. DDR0_06 - (Offset 0x0006)

Initial	Bit	Field	Value	Description
0x0104C823	31:25	—	0000000	Reserved.
	24	WINTRP	1	Support for read commands interrupting write commands.
	23:19	—	00000	Reserved.
	18:16	TWTR	100	DRAM TWTR parameter in cycles.
	15:8	TDLL	11001000	DRAM TDLL parameter in cycles.
	7	—	0	Reserved
	6:0	TRFC	0100011	DRAM TRAS_MIN parameter in cycles.

Table 6-14. DDR0_07 - (Offset 0x0007)

Initial	Bit	Field	Value	Description
0x000D0100	31:25	—	0000000	Reserved.
	24	NCI	0	Issue only REF and PRE commands during DLL initialization of the DRAM devices.
	23:21	—	000	Reserved.
	20:16	TFAW	01101	DRAM TFAW parameter in cycles.
	15:9	—	0000000	Reserved.
	8	ARM	1	Issue refresh on the next command boundary.
	7:1	—	0000000	Reserved.
	0	AREFR	0	Initiate auto-refresh when specified by AUTO_REFRESH_MODE.

Table 6-15. DDR0_08 - (Offset 0x0008)

Initial	Bit	Field	Value	Description
0x02360001	31:27	—	00000	Reserved.
	26:24	WRLAT	010	DRAM WRLAT parameter in cycles.
	23:16	TCPD	00110110	DRAM TCPD parameter in cycles.
	15:9	—	0000000	Reserved.
	8	DQSNEN	0	Single-ended DQS signal from the DRAM
	7:1	—	0000000	Reserved
	0	DDR2	1	DDR2I mode

Table 6-16. DDR0_09 - (Offset 0x0009)

Initial	Bit	Field	Value	Description
0x00011D5F	31:29	—	000	Reserved.
	28:24	OAPDC0	00000	OCD pull-down adjust setting for DRAMs for chip select 0.
	23:18	—	000000	Reserved.
	17:16	RTT0	01	On-Die termination resistance setting for chip select 0 (75 Ohm).
	15	—	0	Reserved.
	14:8	WDSB	0011101	Fraction of a cycle of delay in the write data path in the controller when DLL is being bypassed.
	7	—	0	Reserved.
	6:0	WDS	1011111	Fraction of a cycle of delay in the write data path in the controller.

Table 6-17. DDR0_10 - (Offset 0x0010)

Initial	Bit	Field	Value	Description
0x00000300	31:17	—	000000000 000000	Reserved.
	16	WMDREG	0	Write EMRS data to the DRAMs.
	15:10	—	000000	Reserved.
	9:8	CSMAP	11	Number of active chip selects used in address decoding. Rank 1 installed, rank 0 installed.
	7:5	—	000	DRAM TDLL parameter in cycles.
	4:0	OAPUC0	00000	OCD pull-up adjust setting for DRAMs for chip select 0.

Table 6-18. DDR0_11 - (Offset 0x0011)

Initial	Bit	Field	Value	Description
0x0027C800	31:25	—	0000000	Reserved.
	24	SREFR	0	Disable self-refresh mode.
	23:16	TXSNR	00100111	DRAM TXSNR parameter in cycles.
	15:8	TXSR	11001000	DRAM TXSR parameter in cycles.
	7:0	ARM	00000000	Reserved.

Table 6-19. DDR0_12 - (Offset 0x0012)

Initial	Bit	Field	Value	Description
0x00000003	31:3	—	000000000 000000000 000000000 00	Reserved.
	2:0	TCKE	011	Minimum CKE pulse width in cycles.

Table 6-20. DDR0_14 - (Offset 0x0014)

Initial	Bit	Field	Value	Description
0x00000000	31:25	—	0000000	Reserved.
	24	DLLBYP	0	Normal operational mode.
	23:17	—	0000000	Reserved.
	16	REDUC	0	Standard operation using full 64/72-bit memory bus.
	15:9	—	0000000	Reserved.
	8	RDIM	0	Normal operation
	7:0	—	00000000	Reserved.

Table 6-21. DDR0_17 - (Offset 0x0017)

Initial	Bit	Field	Value	Description
0x19000000	31	—	0	Reserved.
	30:24	DDQSD0	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 0 during reads.
	23:17	—	0000000	Reserved.
	16	DLKREG	0	DLL lock/unlock.
	15	—	0	Reserved.
	14:8	DLLLOK	0000000	Number of delay elements in master DLL lock.
	7:0	—	00000000	Reserved.

Table 6-22. DDR0_18 - (Offset 0x0018)

Initial	Bit	Field	Value	Description
0x19191919	31	—	0	Reserved.
	30:24	DDQSD4	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 4 during reads
	23	—	0	Reserved.
	22:16	DDQSD3	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 3 during reads
	15	—	0	Reserved.
	14:8	DDQSD2	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 2 during reads
	7	—	0	Reserved.
	6:0	DDQSD1	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 1 during reads

Table 6-23. DDR0_19 - (Offset 0x0019)

Initial	31	—	0	Reserved.
0x19191919	30:24	DDQSD8	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 8 during reads
	23	—	0	Reserved.
	22:16	DDQSD7	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 7 during reads
	15	—	0	Reserved.
	14:8	DDQSD6	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 6 during reads
	7	—	0	Reserved.
	6:0	DDQSD5	0011001	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 5 during reads

Table 6-24. DDR0_20 - (Offset 0x0020)

Initial	Bit	Field	Value	Description
0x0B0B0B0B	30:24	DDDB3	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 3 during reads when DLL is being bypassed.
	23	—	0	Reserved.
	22:16	DDDB2	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 2 during reads when DLL is being bypassed.
	15	—	0	Reserved.
	14:8	DDDB1	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 1 during reads when DLL is being bypassed.
	7	—	0	Reserved.
	6:0	DDDB0	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 0 during reads when DLL is being bypassed.

Table 6-25. DDR0_21 - (Offset 0x0021)

Initial	Bit	Field	Value	Description
0x0B0B0B0B	30:24	DDDB7	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 7 during reads when DLL is being bypassed.
	23	—	0	Reserved.
	22:16	DDDB6	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 6 during reads when DLL is being bypassed.
	15	—	0	Reserved.
	14:8	DDDB5	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 5 during reads when DLL is being bypassed.
	7	—	0	Reserved.
	6:0	DDDB4	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 4 during reads when DLL is being bypassed.

Table 6-26. DDR0_22 - (Offset 0x0022)

Initial	Bit	Field	Value	Description
0x00267F0B	31:26	—	000000	Reserved.
	25:24	CTLRAW	00	ECC error checking and correcting control. ECC not being used.
	23	—	0	Reserved.
	22:16	DWQOSB	0100110	Fraction of a cycle to delay the write DQS signal to the DRAMs during writes when DLL is being bypassed.
	15	—	0	Reserved.
	14:8	DQSOSH	01111111	Fraction of a cycle to delay the write DQS signal to the DRAMs during writes when DLL is being bypassed.
	7	—	0	Reserved.
	6:0	DDDB8	0001011	Fraction of a cycle to delay the DQS signal from the DRAMs for slice 8 during reads when DLL is being bypassed.

Table 6-27. DDR0_23 - (Offset 0x0023)

Initial	Bit	Field	Value	Description
0x00000000	31:26	—	000000	Reserved.
	25:24	ORMC0	00	ODT Chip Select 0 map for reads. Determines which chip(s) will have termination when a read occurs on chip 0.
	23:16	ECSYN	00000000	Syndrome for correctable ECC event.
	15:8	EUSYN	00000000	Syndrome for uncorrectable ECC event.
	7:1	—	0000000	Reserved.
	0	FWC	0	Force a write check. XOR XOR_CHECK_BITS with ECC code and write to memory. No action.

Table 6-28. DDR0_24 - (Offset 0x0024)

Initial	Bit	Field	Value	Description
0x01010002	31:26	—	000000	Reserved.
	25:24	RTTPT	01	Set termination resistance in controller pads. 75 Ohm.
	23:18	—	000000	Reserved.
	17:16	OWMC1	01	ODT Chip Select 1 map for writes. Determines which chip(s) will have termination when a write occurs on chip 1.
	15:10	—	000000	Reserved.
	9:8	ORMC1	00	ODT Chip Select 1 map for writes. Determines which chip(s) will have termination when a read occurs on chip 1.
	7:2	—	000000	Reserved.
	1:0	OWMC0	10	ODT Chip Select 0 map for writes. Determines which chip(s) will have termination when a write occurs on chip. CS1 will have active ODT termination when CSx is performing a write.

Table 6-29. DDR0_26 - (Offset 0x0026)

Initial	Bit	Field	Value	Description
0x5B260181	31:16	TRAS_MAX	0101101100100110	DRAM TRAS_MAX parameter in cycles.
	15:14	—	00	Reserved.
	13:0	TREF	0000011000001	DRAM TREF parameter in cycles.

Table 6-30. DDR0_27 - (Offset 0x0027)

Initial	Bit	Field	Value	Description
0x0000682B	31:30	—	00	Reserved.
	29:16	EMRSDT	0000000000000	Extended mode register data written during initialization or when WRITE_MODEREG is 1.
	15:0	TINIT	0110100000101011	DRAM TINIT parameter in cycles.

Table 6-31. DDR0_28 - (Offset 0x0028)

Initial	Bit	Field	Value	Description
0x00000000	31:30	—	00	Reserved.
	29:16	EMRS3D	0000000000000	EMRS3 Data written during DDRII initialization.
	15:14	—	00	Reserved.
	13:0	EMRS2D	0000000000000	EMRS2 Data written during DDRII initialization.

Table 6-32. DDR0_31 - (Offset 0x0031)

Initial	Bit	Field	Value	Description
0x00000000	31:16	—	0000000000000000	Reserved.
	15:0	XORCB	0000000000000000	Value to XOR with generated ECC codes for forced write check.

Table 6-33. DDR0_42 - (Offset 0x0042)

Initial	Bit	Field	Value	Description
0x01000006	26:24	APIN	001	Difference between the maximum number of address pins available (14) and the number being used.
	3:0	CLGATE	0110	Adjusts data capture gate open by half-cycles. 3 cycles.

Table 6-34. DDR0_43 - (Offset 0x0043)

Initial	Bit	Field	Value	Description
0x050A0200	31:27	—	00000	Reserved.
	26:24	TWR	101	DRAM TWR parameter in cycles.
	23:20	—	0000	Reserved.
	19:16	APREBIT	1010	Location of the automatic precharge bit in the DRAM address.
	15:11	—	00000	Reserved.
	10:8	COLSIZ	010	Difference between maximum number of column pins available(12) and number being used.
	7:1	—	0000000	Reserved.
	0	BNK8	0	Number of banks on the DRAM(s). Memory devices have 4 banks.

Table 6-35. DDR0_44 - (Offset 0x0044)

Initial	Bit	Field	Value	Description
0x00000005	31:8	—	000000000000000000000000	Reserved.
	7:0	CLGATE	00000101	DRAM TRCD parameter in cycles.

Table 6-36. DDR0_02 - (Offset 0x0002)

Initial	Bit	Field	Value	Description
0x0000001	31:26	—	000000	Reserved.
	25:24	MAXCS	00	Maximum number of chip selects available
	23:20	—	0000	Reserved.
	19:16	MAXCOL	0000	Maximum width of column address in DRAMs
	15:12	—	0000	Reserved.
	11:8	MAXROW	0000	Maximum width of memory address bus (0 row bits)
	7:1	—	0000000	Reserved.
	0	START	1	Controller is in active mode

I2C Devices and Addressing

Chapter 7

The evaluation board has a total of four devices that access the I2C bus. These three devices are a serial temperature and thermal monitor (STTM), a serial EEPROM (SEP) for boot configuration with 66 MHz PCI clocking, a serial EEPROM (SEP) for boot configuration with 33 MHz PCI clocking and a serial EEPROM (SEP) for firmware keys.

Table 7-1. I2C Address Map

Device	Function	I2C Addressing
STTM	Serial temperature and thermal monitor	STTM_ADD signal Float = 1001 000 (**hard-coded default**) GND= 1001 001 VDD = 1001 010
SEP	Boot configuration (66 MHz PCI)	0xA4 - A7 for 4K device (512 x 8)
SEP	Boot configuration (33 MHz PCI)	0xA4 - A7 for 4K device (512 x 8)
SEP	Firmware keys	0xA8 - AB for 4K device (512 x 8)

There are two I2C ports on the evaluation board. Port 0 of the I2C is used by the three onboard EEPROM and the STTM. Port 1 can be configured as a second I2C port or SPI port and is accessible on a 1 x 5 header (P4).

STTM Device

The STTM address is controlled by a single signal, STTM_ADD, from the CPLD. This signal has three states, Float, GND and VDD. Other address are available, but a different part number would have needed to be used. Refer to the Analog Devices AD7414 data sheet for details.

EEPROM (SEP)

The two boot configuration SEPs are identical and reside at the same address (0xA4). Only one boot configuration SEP can access the I2C circuit at any given time. Access is controlled via a switch part (U30) and the M66EN signal. When the M66EN signal is asserted, the user will have access to the SEP configured with 66 MHz PCI clocking. When the M66EN signal is not asserted, the user will have access to the SEP configured with 33 MHz PCI clocking. The configuration settings in both SEPs need to be set up separately by the user.

The evaluation board is also populated with a switch (SW2) that allows the user to override an asserted M66EN signal and force the board into 33 MHz PCI operation. The settings for this switch can be found in Table 4-3.

Restoring the Boot EEPROM

The procedure for restoring the boot EEPROM (SEP) is as follows:

NOTE: There should be no PCI card in the PCI slot when attempting this procedure.

1. Power down the board.
2. Set SW2 (CONFIG) as:

   Position 1: 0 (ON)
   Position 2: 1 (OFF)
   Position 3: 0 (ON)
   Position 4: 1 (OFF)

   NOTE: on = closed position will read back a logic 0 in the status register.
   off = open position will read back a logic 1 in the status register.

3. Remove jumper J2 if populated.
4. Power up the board. The board should boot normally to the u-boot prompt.
5. Use the **mm** command to write the boot EEPROM values to a RAM location, and then use the **eeprom** command to write those values to the SEP. Refer to Table 7-2 for the values to program into the first boot SEP (33 MHz PCI) depending on the processor speed and type of boot operation. For example, give the following commands to reprogram the SEP:

   => **mm 0x100000 ENTER**
   00100000: 00000000 ? **0x87788252 ENTER**
   00100004: 00000000 ? **0x0947A030 ENTER**
   00100008: 00000000 ? **0x40082350 ENTER**
   0010000c: 00000000 ? **0x0D050000 ENTER**
   00100010: 00000000 ? **. ENTER**
   => **eeprom write 0x52 0x100000 0x0 0x10 ENTER**

Table 7-2. Boot EEPROM Settings (33 MHz PCI)

Offset	533 MHz (NOR Boot)	667 MHz (NOR Boot)	533 MHz (NAND Boot)	667 MHz (NAND Boot)
0x00	0x87788252	0x8778A252	0x87788252	0x8778A252
0x04	0x0947A030	0x09C7A030	0x0947D010	0x09C7D010
0x08	0x40082350	0x40082350	0xA0682358	0xA0682358
0x0C	0x0D050000	0x0D050000	0x0D050000	0x0D050000

6. Set SW2 (CONFIG) as:

   Position 1: 0 (ON)
   Position 2: 1 (OFF)
   Position 3: 0 (ON)
   Position 4: 0 (ON)

   NOTE: on = closed position will read back a logic 0 in the status register.
   off = open position will read back a logic 1 in the status register.

7. Use the **mm** command to write the boot EEPROM values to a RAM location, and then use the **eeprom** command to write those values to the SEP. Refer to

Table 7-3 for the values to program into the second boot SEP (66 MHz PCI) depending on the processor speed and type of boot operation. For example, give the following commands to reprogram the SEP:

=> **mm 0x100000 ENTER**
00100000: 00000000 ? **0x87788252 ENTER**
00100004: 00000000 ? **0x0957A030 ENTER**
00100008: 00000000 ? **0x40082350 ENTER**
0010000c: 00000000 ? **0x0D050000 ENTER**
00100010: 00000000 ? **. ENTER**
=> **eeprom write 0x52 0x100000 0x0 0x10 ENTER**

Table 7-3. Boot EEPROM Settings (66 MHz PCI)

Offset	533 MHz (NOR Boot)	667 MHz (NOR Boot)	533 MHz (NAND Boot)	667 MHz (NAND Boot)
0x00	0x87788252	0x8778A252	0x87788252	0x8778A252
0x04	0x0957A030	0x09D7A030	0x0957D010	0x09D7D010
0x08	0x40082350	0x40082350	0xA0682358	0xA0682358
0x0C	0x0D050000	0x0D050000	0x0D050000	0x0D050000

8. Remove power from the board.
9. Set SW2 (CONFIG) as:

   Position 1: 1 (OFF)
   Position 2: 1 (OFF)
   Position 3: 1 (OFF)
   Position 4: 1 (OFF)

   NOTE: on = closed position will read back a logic 0 in the status register.
   off = open position will read back a logic 1 in the status register.

10. If booting from NAND FLASH, install jumper J2.
11. Power up the board.

STTM Format and Interface Structure

The driver for the STTM sets the interrupt out for low true operation. An interrupt is triggered via the STTM_ALERT signal on the IRQ3 pin of the PPC440EPx or PPC440GRx processor and is disabled when u-boot is not testing the STTM. The driver returns the temperature of the device and also a calibrated temperature for reporting ambient air temperature. The calibration parameter is programmed into the SEP and is used to extrapolate ambient air temperature.

Interrupt Structure

Chapter 8

All on-board interrupts should be programmed active low on the PPC440EPx or PPC440GRx IRQ pins. Table 8-1 identifies the possible IRQ lines that an onboard device or external peripheral could send to the PPC440EPx or PPC440GRx. IRQ0-9 have programmable polarity. For further information on this, refer to the ***PPC440EPx*** or ***PPC440GRx AMCC User Manuals***.

Table 8-1. Interrupts

IRQ #	Signal
IRQ0	GETH0_IRQ
IRQ1	GETH1_IRQ
IRQ2	$\overline{\text{PCI\_INTA}}$
IRQ3	STTM_ALERT
IRQ4	GPIO44
IRQ5	GND
IRQ6	GPIO45
IRQ7	GPIO46
IRQ8	GPIO47
IRQ9	GPIO48

Mechanical Dimensions

Appendix A

This appendix contains mechanical dimension drawings needed to design the evaluation board into a product. Figures A-1, A-2 and A-3 show the dimensions for the evaluation board.

NOTES:

1. The dimensions in this document are believed correct, but if this unit is to be placed into a housing that has cut outs, an actual unit must be procured to verify all required connector cut outs. In addition, the vendor's data sheets for the connectors should be referenced to determine the tolerances of the connectors.

2. The pin headers can optionally be populated with either straight pins or right-angle pins. Figure A-3 shows the pin dimensions. The right-angle pins extent 0.33 inches (8.4 millimeters) past the edge of the board as shown in the figure.

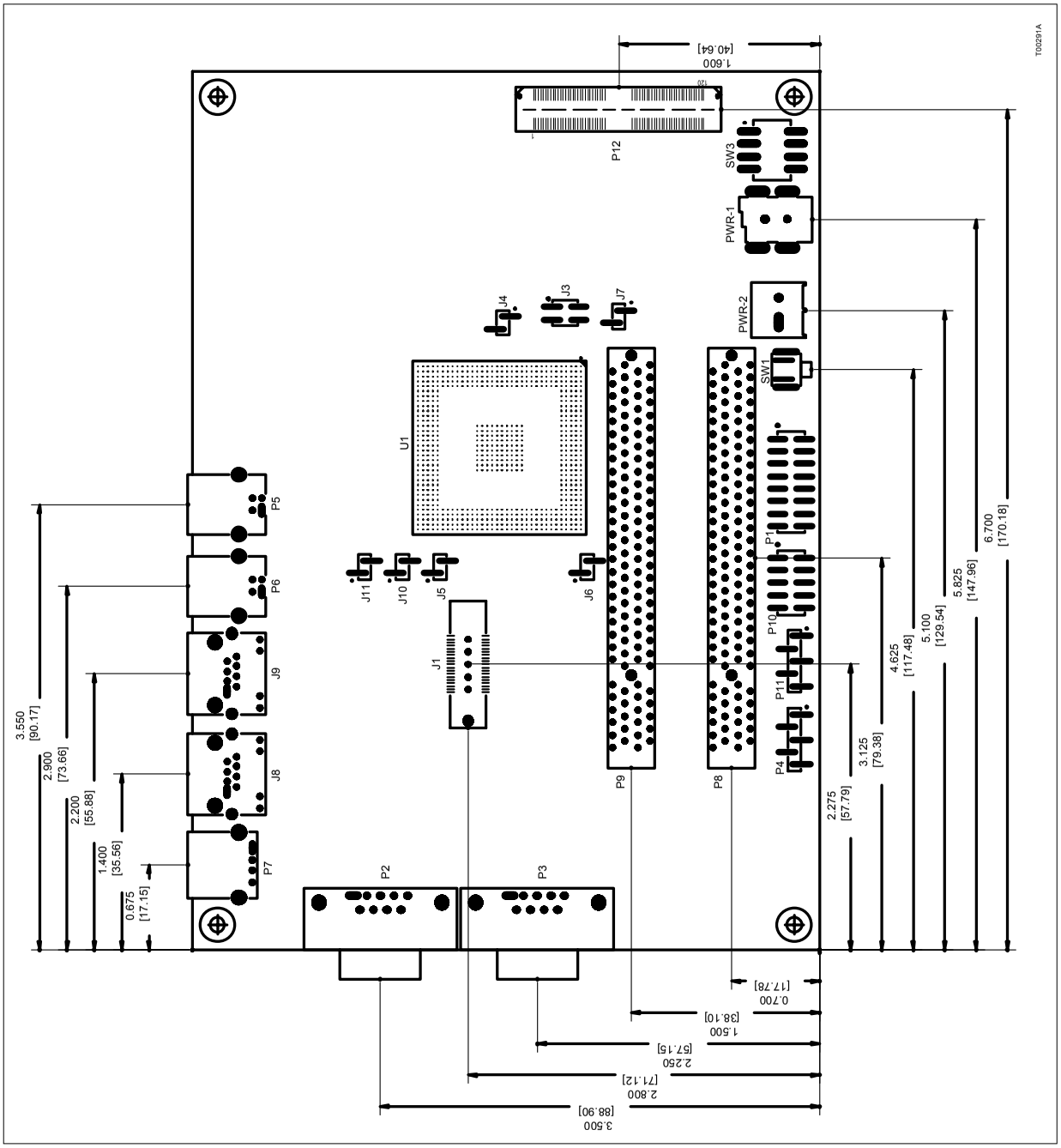

Figure A-1. Evaluation Board - Front Mechanical

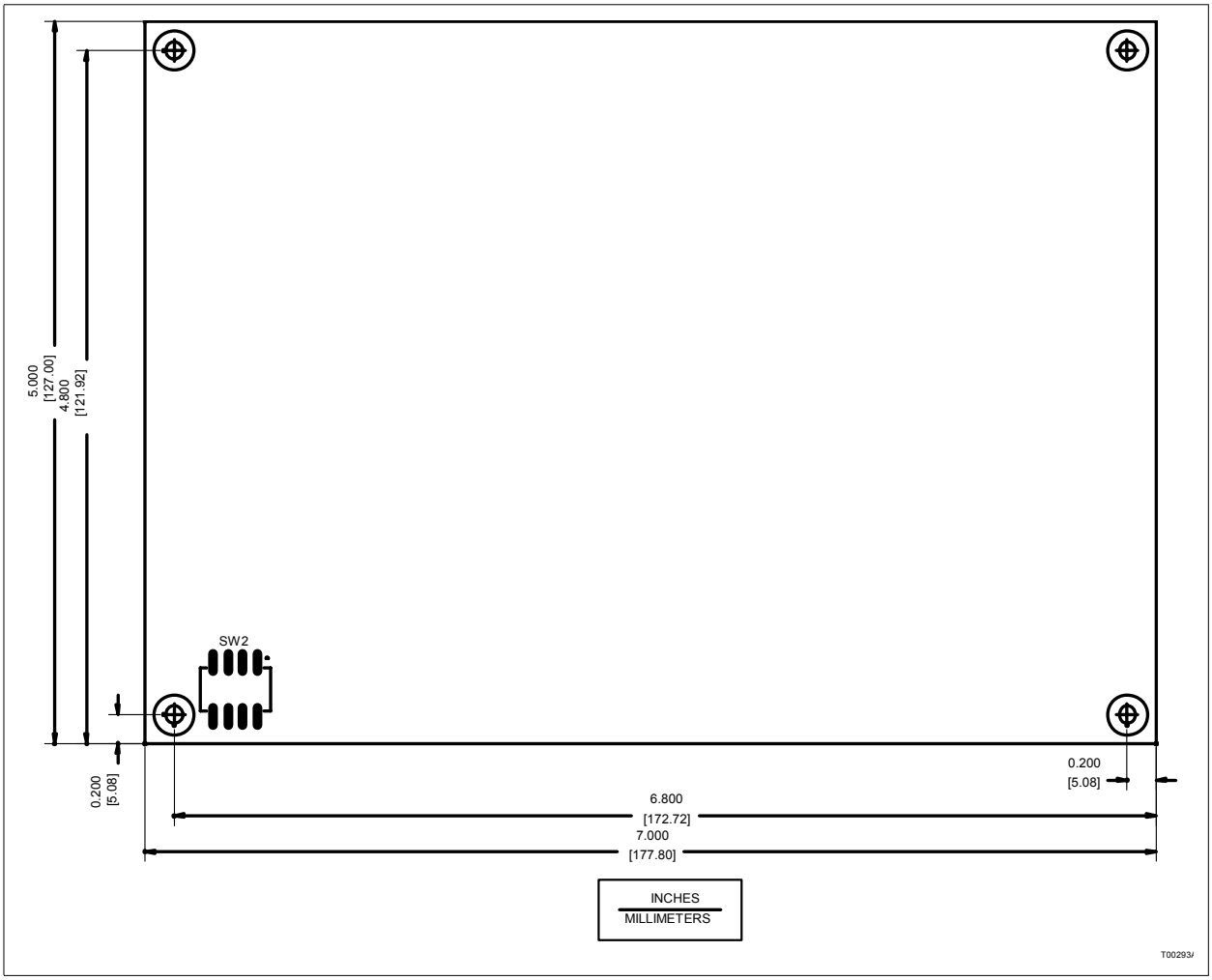

Figure A-2. Evaluation Board - Back Mechanicals

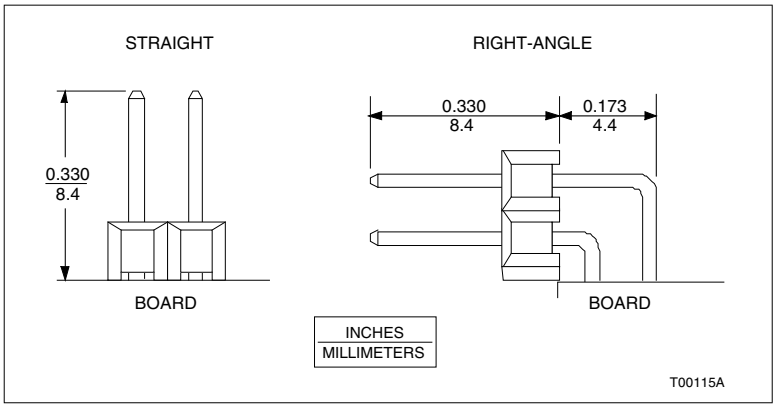

Figure A-3. Straight and Right-Angle Pin Dimensions

Embedded Planet
4760 Richmond Road, Suite 400
Warrensville Heights, OH 44128
www.embeddedplanet.com

Phone: 216.245.4180
Fax: 216.292.0561

Form P5010000069SB01 Litho in U.S.A. May2007