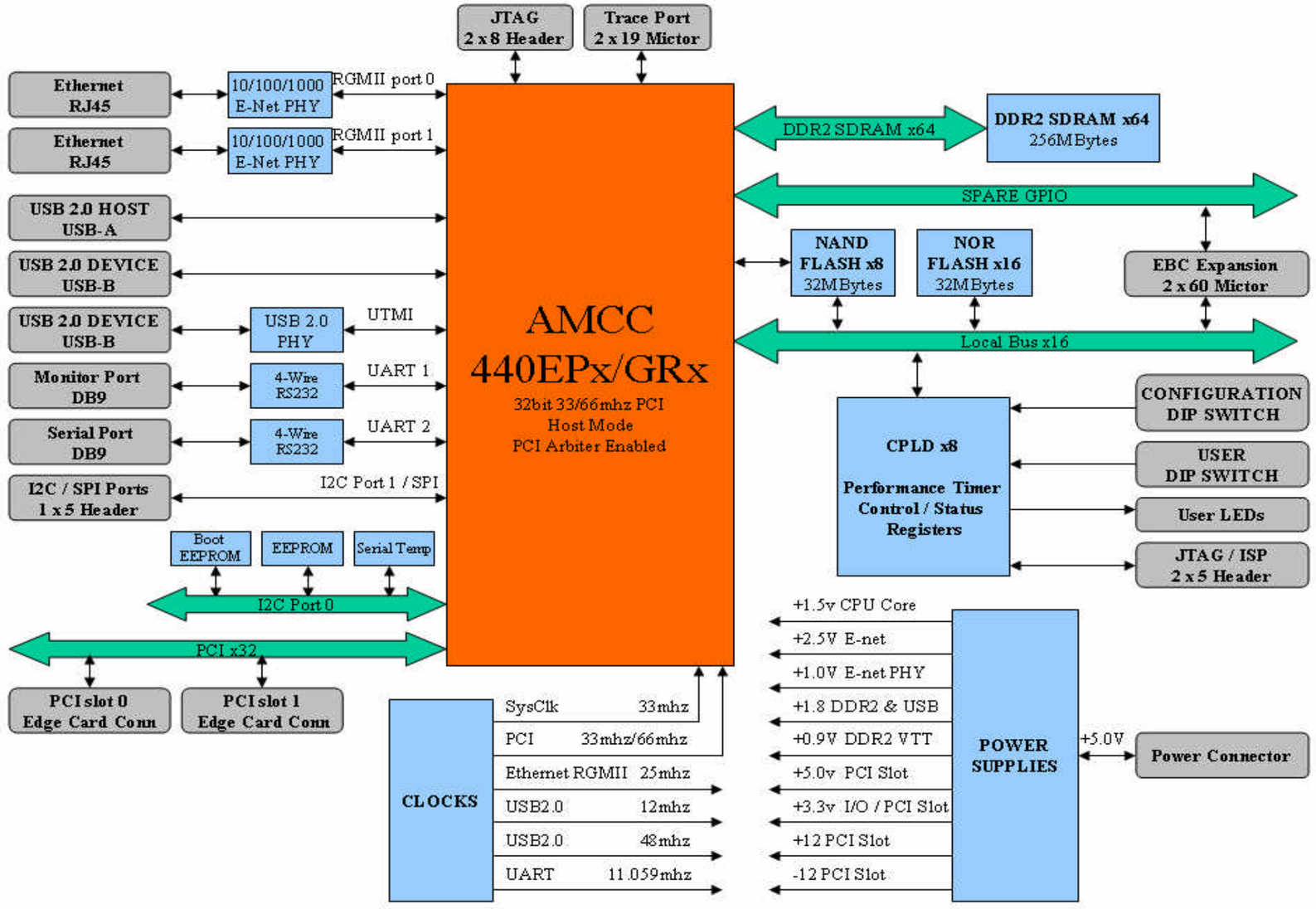
DES0211
EP440Cx



PAGE INDEX -

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Page Name: Title_Block Diagram
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Thursday, September 07, 2006 | Sheet 1 of 11

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "+1.5V"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "+1.8V"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "+2.5V"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "+3.3V"

Place components close to CPU

Place components close to CPU

Place components close to CPU

U1A
TE-PBGA680
44OEPx/GRx
POWER

AP24 AVdd
AP25 AGND
AP28 EAVdd
AP27 EAGND

+5.0 V

PWR-1
PJ-002AH-SMT

PWR-2
1x2 5mm TH
Term Block

FH3 SMT 10x5mm 5A Holder
FH1 SMT 10x5mm 10A Holder
FH2 SMT 10x5mm 10A Holder

+5V_VIN

Alternate power input terminal
Two 10A fuses result in 16A rating

Bulk Decoupling

CPU Core by-pass caps place as close to CPU VDD pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

+1.8 V

Place all components within this block close together

+1.5 V

~2.9Amp

~3.6Amp

U2
LTC3736EUF
QFN24

Q1A Si7540DP SO-8
Q1B Si7540DP SO-8
Q2A Si7540DP SO-8
Q2B Si7540DP SO-8

L20 1.5uH IHLP-2525CZ-01
L21 1.5uH IHLP-2525CZ-01

PWR_OUT1
PWR_OUT2

VOUT= 0.6v(1+R1/R2)

3,4,11 PWR_GOOD

Place these 4 caps close to DDR parts

Bulk Decoupling

CPU Core by-pass caps place as close to CPU OVdd pins as possible

+0.9 V

Place all components within this block close together

U3
MSOP10
TPS51100

DDR_VREF_+0.9V
Use 25mil trace

VTT Island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

NOTE: The analog grounds, GND_U2 and GND_U3, must each be tied to the digital ground, GND, at a single point, preferably very close to the IC.

Each Analog GND tied to Digital GND at a single point.

4 mounting holes

H1 7mmP 3mmD P Test
H2 7mmP 3mmD P Test
H3 7mmP 3mmD P Test
H4 7mmP 3mmD P Test

APPROVAL	DATE

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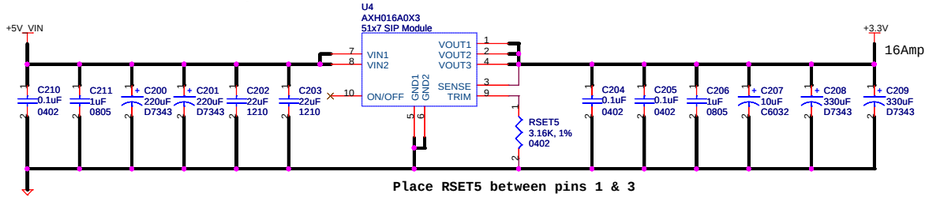
Page Name: Power: +1.5V, +1.8V, +0.9V
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Thursday, September 07, 2006 | Sheet 2 of 11

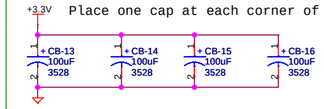
Place all components within
this block close together

+3.3 V



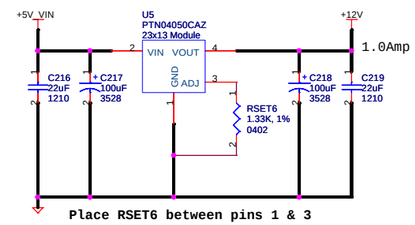
Place RSET5 between pins 1 & 3

Place one cap at each corner of the PCB



Place all components within
this block close together

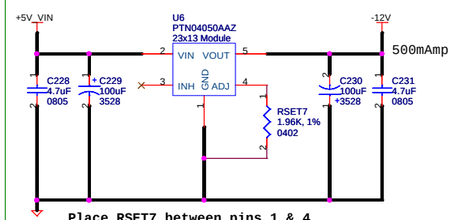
+12 V



Place RSET6 between pins 1 & 3

Place all components within
this block close together

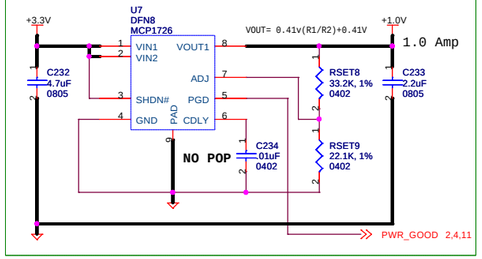
-12 V



Place RSET7 between pins 1 & 4

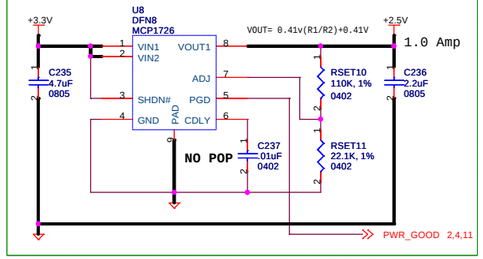
Place all components within
this block close together

+1.0 V



Place all components within
this block close together

+2.5 V



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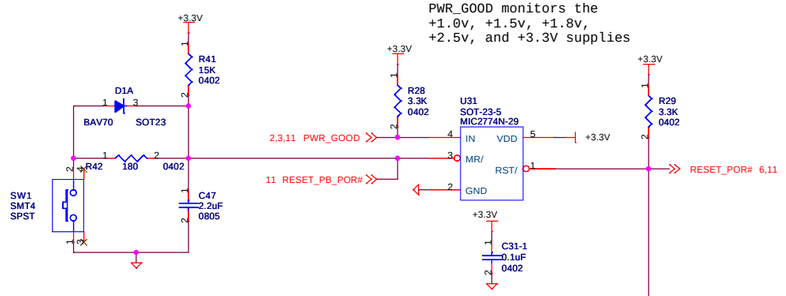
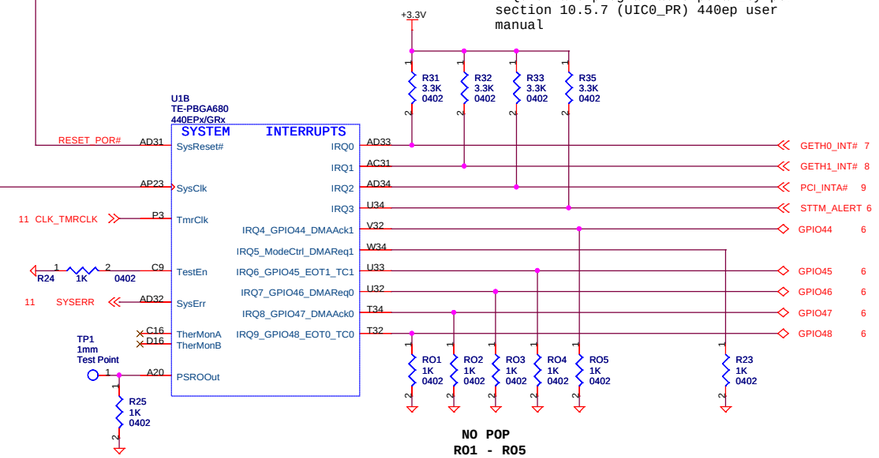
Page Name	Power: +1.0V, +2.5V, +3.3V, +12V, -12V
Title	Des0211_11
Size: Custom / Document Number	Des0211_11_sch_10
Rev	1.0
Date: Thursday, September 07, 2006	Sheet 3 of 11

PWR_GOOD monitors the
+1.0v, +1.5v, +1.8v,
+2.5v, and +3.3V supplies



IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

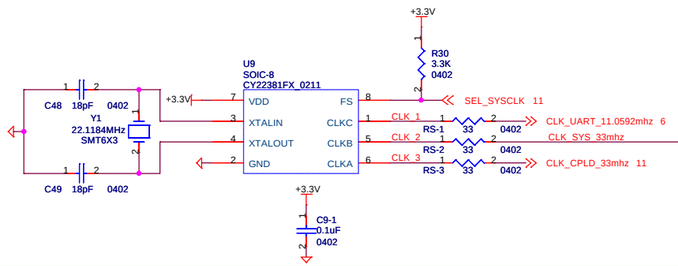


NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:

CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz



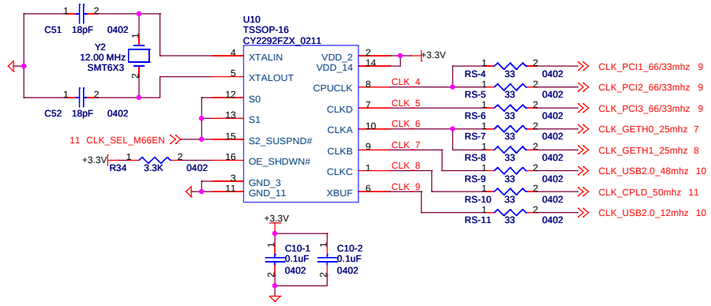
Critical Placement and Route
Clock Rules:

Clock Rules:

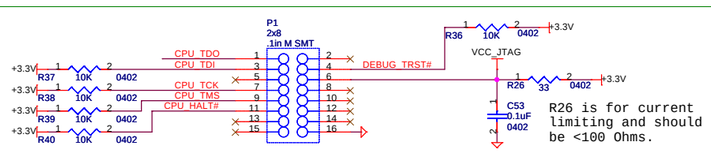
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"

CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz

CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

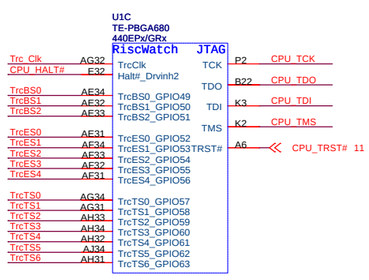


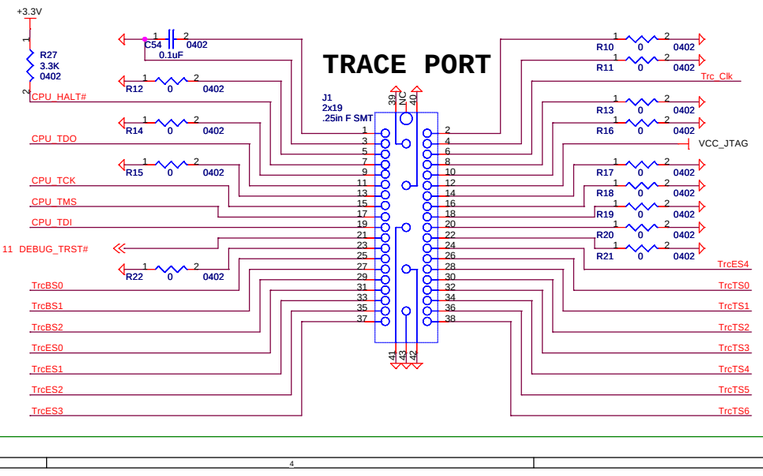
TRACE & JTAG CONNECTORS



R26 is for current limiting and should be <100 Ohms.

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4





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Page Name: Resets_Clocking_IRQs_Debug
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Wednesday, September 13, 2006 | Sheet 4 of 11

DDR_DQ[0..63]

Critical Placement:
Place Series Resistors as close to DDR as possible

Critical Placement:
Place Series Resistors as close to DDR as possible

U1D
TE-PBGA680
440EPx/GRx
DDR SDRAM

DDR by-pass caps place as close to DDR power pins as possible (1 cap for every 2 pins)

DDR by-pass caps place as close to DDR power pins as possible (1 cap for every 2 pins)

DDR by-pass caps place as close to DDR power pins as possible (1 cap for every 2 pins)

U11 FBGA92 64Mbx16 DDR2

U12 FBGA92 64Mbx16 DDR2

U13 FBGA92 64Mbx16 DDR2

NO POP CAP
Critical Placement: Place as close as possible to pins M8 and N8 of device

500ps Loop

Place parts as close to CPU as possible

Critical Placement

U32 OFN40 9x877

- Route all DDR clocks as differential pairs
- The trace length of DDR_CLKOUT must be slightly longer than the addr,cmd,ctrl signal nets
- DDR_CLKFB trace length must equal the other DDR_CLK#s

Critical Placement:
Place Compensation Caps at Series Res. end of TL0 segment per Layout Example

Critical Placement:
Place Load-Matching Caps at DDR end of net (TL6) per Layout Example

NO POP

Critical Placement:
Place Parallel Termination at DDR end of net (TL5) per Layout Example

DDR by-pass caps place as close to DDR power pins as possible (1 cap for every 2 pins)

U14 FBGA92 64Mbx16 DDR2

CRITICAL PLACEMENT AND ROUTING:
All Components, and signals on this page have very tight and critical routing and placement parameters:

(IDEAL Layout)
All clocks = each other = data lines = control = address
In other words all signals equal each other.

Place series resistors and compensation capacitors close to the DDR2 devices (TL1 is much smaller than TL0). Place termination resistors on the top layer at VTT island, at end of bus. Use wide island trace to increase current capacity (3A).

Route DDR2 signals only on layers that are directly adjacent to the designated reference plane: GND for DQ,DM,DQS; VDD for ADD.

Route each 10-bit byte lane of the data group (DQ, DQS, and DM) on the same layers with matched trace lengths (within +/- 25 mils of the respective strobe, DQS). Vias and BGA breakout patterns should be included in the analysis of each individual trace length. Include 1.6mm net length per via.

To help reduce crosstalk, data and data strobes should be isolated from the address and command signals. This is accomplished by routing different signal types on separate layers of the printed circuit board.

Total trace lengths for any signal, CPU to DRAM must not exceed 100 mm. Separate data and control nets by a minimum of 0.5 mm to minimize crosstalk.

LAYOUT EXAMPLE

CPU Addr Nets

TL0 >> TL1

TL0 R-SERIES TL1 C-Comp GND

TL2 TL3 TL4 DDR1

TL2 TL3 TL4 DDR2 R-TERM VTT ISLAND

TL5 C-Load Matching GND

TL2 TL3 TL4 DDR3

TL3 TL4 DDR4

Refer to:
JEDEC "PC2-4200/PC2-3200 DDR2 Unbuffered MicroDIMM Reference Design Specification" Rev 0.5 4/26/04

Micron TN-47-01 "DDR2 Design Guide for Two-DIMM System"

DDR devices should be placed and routed in an analogous fashion to optimize signal fan-out.

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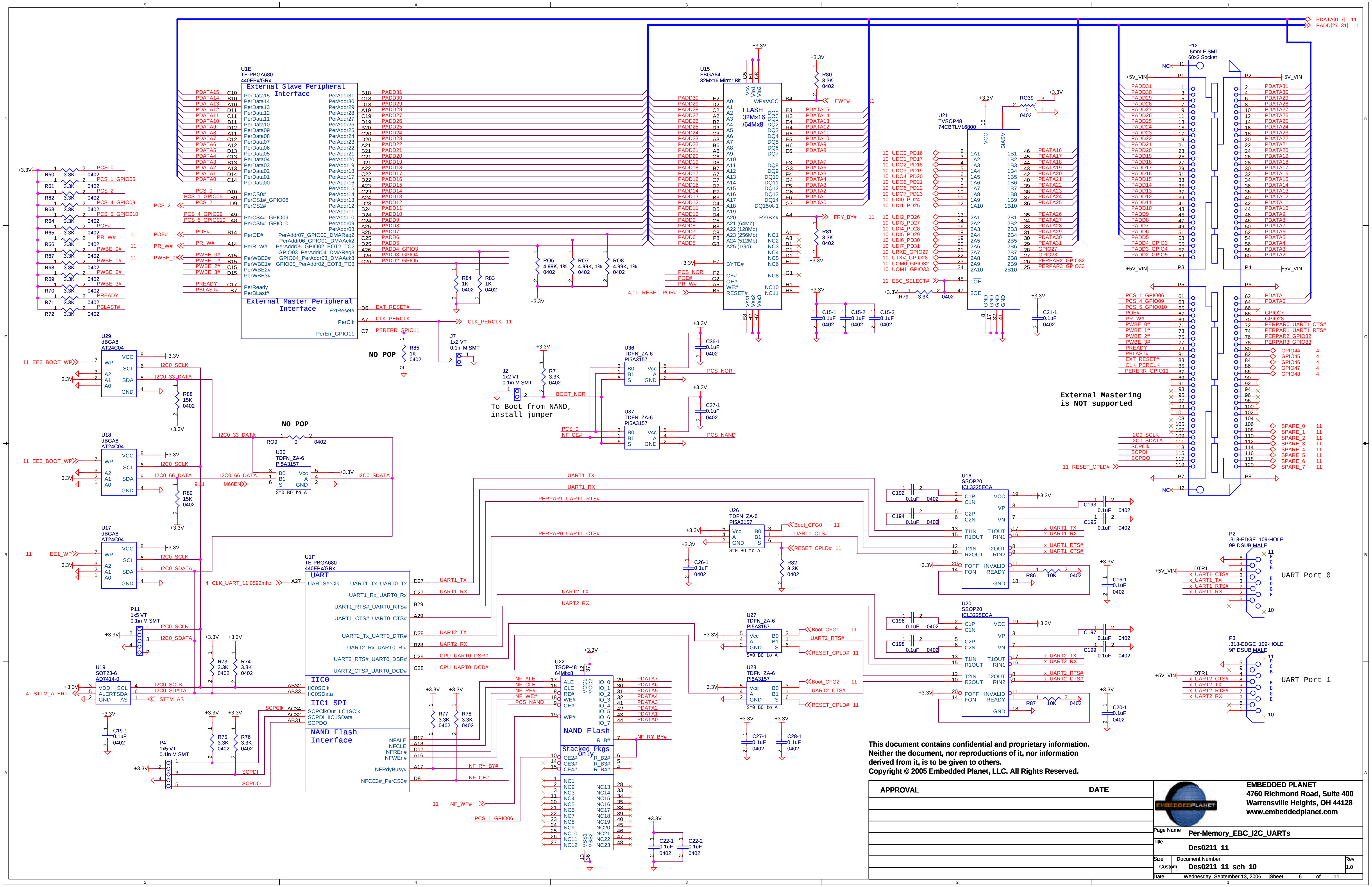
Page Name: DDR-Memory
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Wednesday, September 13, 2006 | Sheet 5 of 11



APPROVAL	DATE

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Page Name	Per-Memory_EBC_I2C_UARTs		
Title	Des0211_11		
Size: Custom	Document Number: Des0211_11_sch_10		Rev: 1.0
Date: Wednesday, September 13, 2006	Sheet 6 of 11		

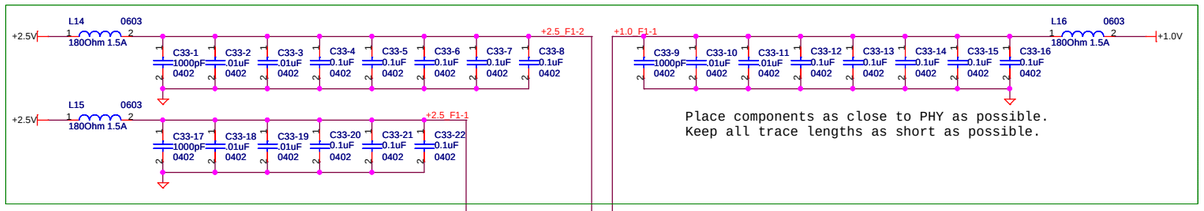
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.

It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.

Minimize the number of via on the RGMII lines to minimize timing skew.

Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.



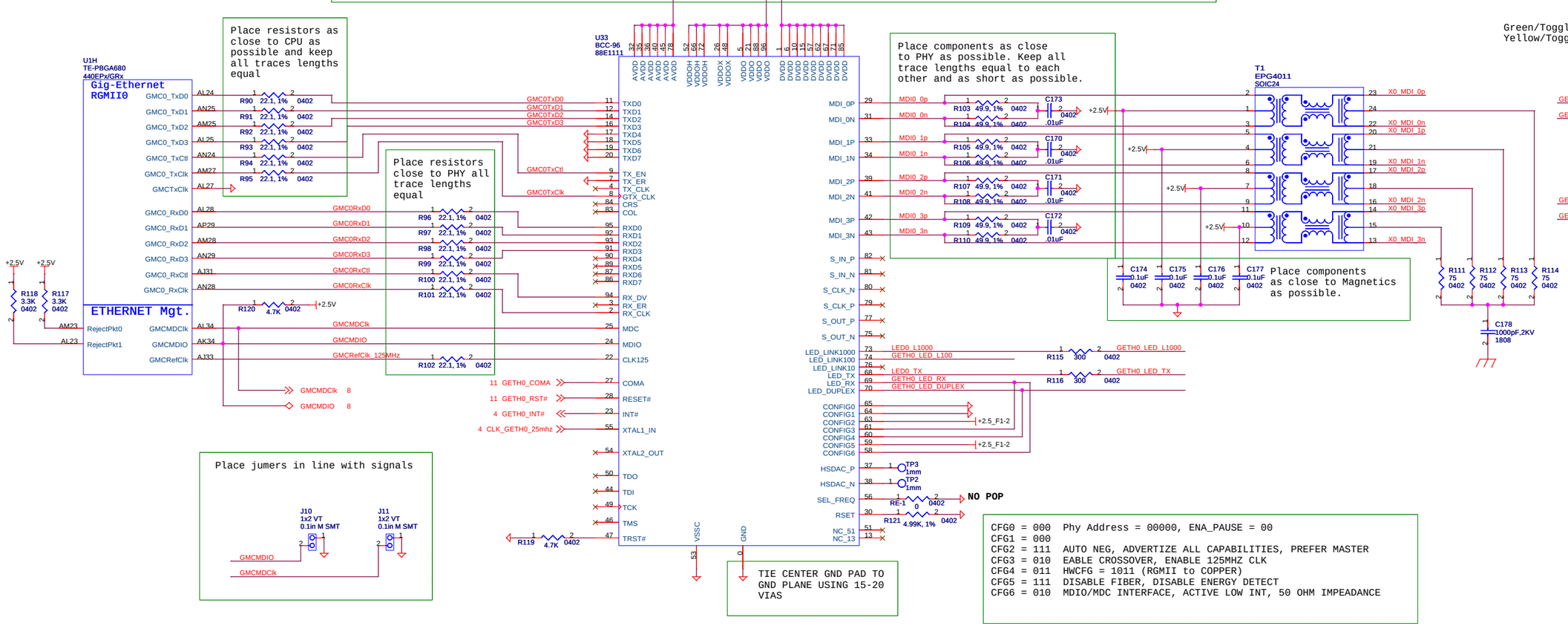
Ethernet LEDs
Top LED = SPEED/LINK
(PHY Reg 24.5:3 = '111')
Green = 1000
Yellow = 100
Off = 10
Bottom LED = DUPLEX/ACTIVITY
(Phy reg 24.2 & 7 = '10', and Phy Reg 24.6 & 0 = '11')
Green/Toggle = Full Duplex/TX or RX activity
Yellow/Toggle = Half Duplex/TX or RX activity

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place components as close to Magnetics as possible.



Place jumers in line with signals

TIE CENTER GND PAD TO GND PLANE USING 15-20 VIAS

```
CFG0 = 000  Phy Address = 00000, ENA_PAUSE = 00
CFG1 = 000
CFG2 = 111  AUTO NEG, ADVERTIZE ALL CAPABILITIES, PREFER MASTER
CFG3 = 010  EABLE CROSSOVER, ENABLE 125MHZ CLK
CFG4 = 011  HWCFG = 1011 (RGMII to COPPER)
CFG5 = 111  DISABLE FIBER, DISABLE ENERGY DETECT
CFG6 = 010  MDIO/MDC INTERFACE, ACTIVE LOW INT, 50 OHM IMPEADANCE
```

Marvell 88e1111 data sheet section 2.4.1

PIN to CONSTANT MAPPING

VDDO	= 111
LED_LINK_10	= 110
LED_LINK_100	= 101
LED_LINK_1000	= 100
LED_DUPLEX	= 011
LED_RX	= 010
LED_TX	= 001
VSS	= 000

PIN to CONFIGURATION MAPPING

PIN	BIT2	BIT1	BIT0
CONFIG0	PHYADR2	PHYADR1	PHYADR0
CONFIG1	ENA_PAUSE	PHYADR4	PHYADR3
CONFIG2	ANEG3	ANEG2	ANGE1
CONFIG3	ANEG0	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE2	HWCFG_MODE1	HWCFG_MODE0
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE3
CONFIG6	SEL_TWSI	INT_POL	75/50 ohm

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Page Name: Gig-Ethernet 0
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Thursday, September 07, 2006 | Sheet 7 of 11

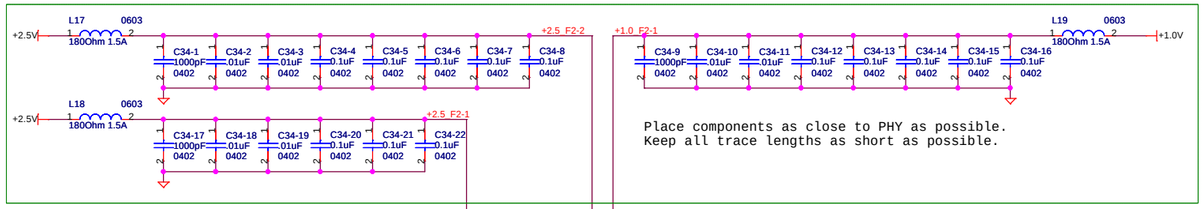
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.

It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.

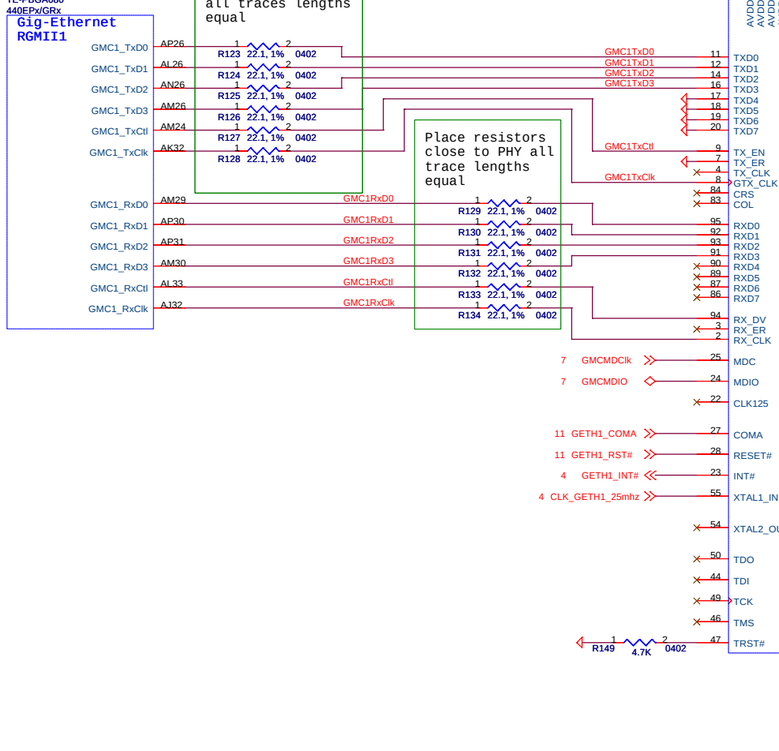
Minimize the number of via on the RGMII lines to minimize timing skew.

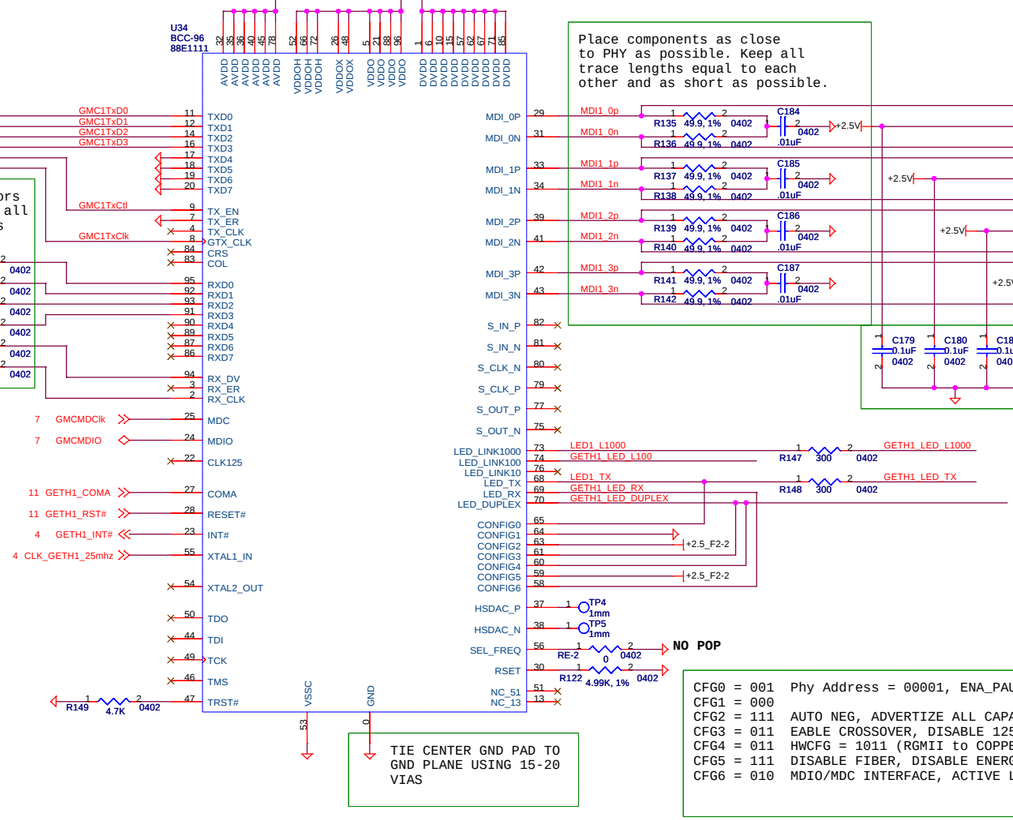
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.



Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal





Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Ethernet LEDs
Top LED = SPEED/LINK
(PHY Reg 24.5:3 = '111')
Green = 1000
Yellow = 100
Off = 10
Bottom LED = DUPLEX/ACTIVITY
(Phy reg 24.2 & 7 = '10', and Phy Reg 24.6 & 0 = '11')
Green/Toggle = Full Duplex/TX or RX activity
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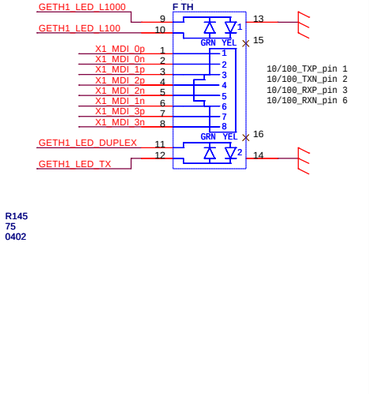

Marvell 88e1111 data sheet section 2.4.1

PIN to CONSTANT MAPPING

VDDO	= 111
LED_LINK_10	= 110
LED_LINK_100	= 101
LED_LINK_1000	= 100
LED_DUPLEX	= 011
LED_RX	= 010
LED_TX	= 001
VSS	= 000

PIN to CONFIGURATION MAPPING

PIN	BIT2	BIT1	BIT0
CONFIG0	PHYADR2	PHYADR1	PHYADR0
CONFIG1	ENA_PAUSE	PHYADR4	PHYADR3
CONFIG2	ANEG3	ANEG2	ANGE1
CONFIG3	ANEG0	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE2	HWCFG_MODE1	HWCFG_MODE0
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE3
CONFIG6	SEL_TWSI	INT_POL	75/50 ohm

TIE CENTER GND PAD TO GND PLANE USING 15-20 VIAS

```
CFG0 = 001  Phy Address = 00001, ENA_PAUSE = 00
CFG1 = 000
CFG2 = 111  AUTO NEG, ADVERTIZE ALL CAPABILITIES, PREFER MASTER
CFG3 = 011  EABLE CROSSOVER, DISABLE 125MHZ CLK
CFG4 = 011  HWCFG = 1011 (RGMII to COPPER)
CFG5 = 111  DISABLE FIBER, DISABLE ENERGY DETECT
CFG6 = 010  MDIO/MDC INTERFACE, ACTIVE LOW INT, 50 OHM IMPEADANCE
```


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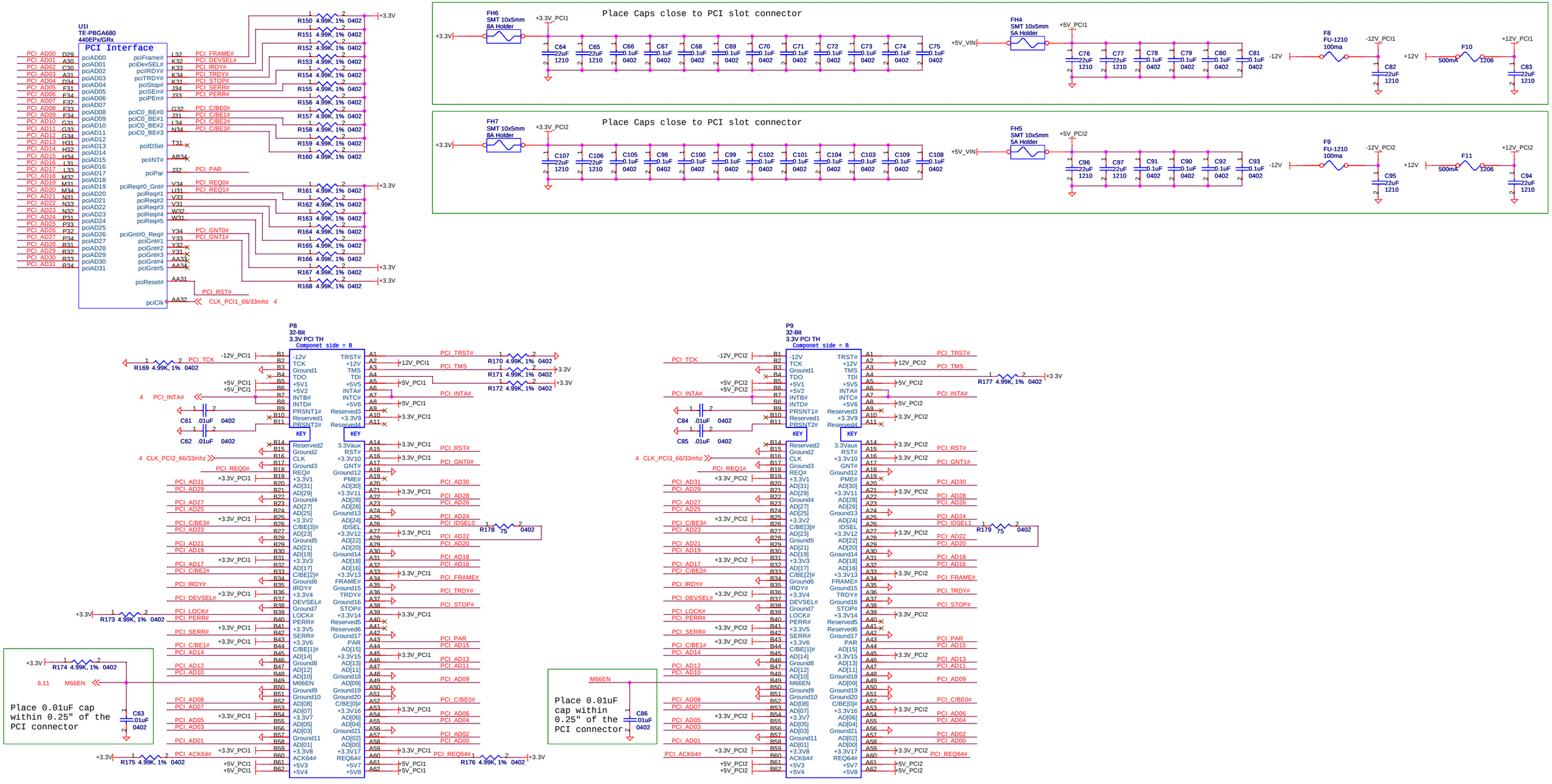
Page Name	Gig-Ethernet 1
Title	Des0211_11
Size / Document Number	Custom / Des0211_11_sch_10
Rev	1.0
Date:	Thursday, September 07, 2006
Sheet	8 of 11



Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

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Page Name: PCI
Title: Des0211_11
Size: Custom | Document Number: Des0211_11_sch_10 | Rev: 1.0
Date: Thursday, September 07, 2006 | Sheet 9 of 11

U23
TVSOP48
74CBTLV16800

U1G
TE-PBGA680
440EPx/GRx

USB 2.0 DEVICE

USB 2.0 PHY
HOST/DEVICE

U24
GT3250-ABZJ
QFN-56 (8mm x 8mm)

RO40 0 0402

RO34 NO POP

RO30: [1:2] for 440EPx
[3:2] for 440GRx

Place parts as close to USB PHY as possible

Place parts close to USB PHY

NO POP

Place SP1 very close to P5

Critical Placement

Place SP2 very close to P6

Critical Placement

Place SP3 very close to P7

Critical Placement

RO resistors for 440GRx only

Place these resistors as close as possible to the CPU's pin

Keep all other high speed signals away from these traces

NO POP for 440EPx

APPROVAL DATE

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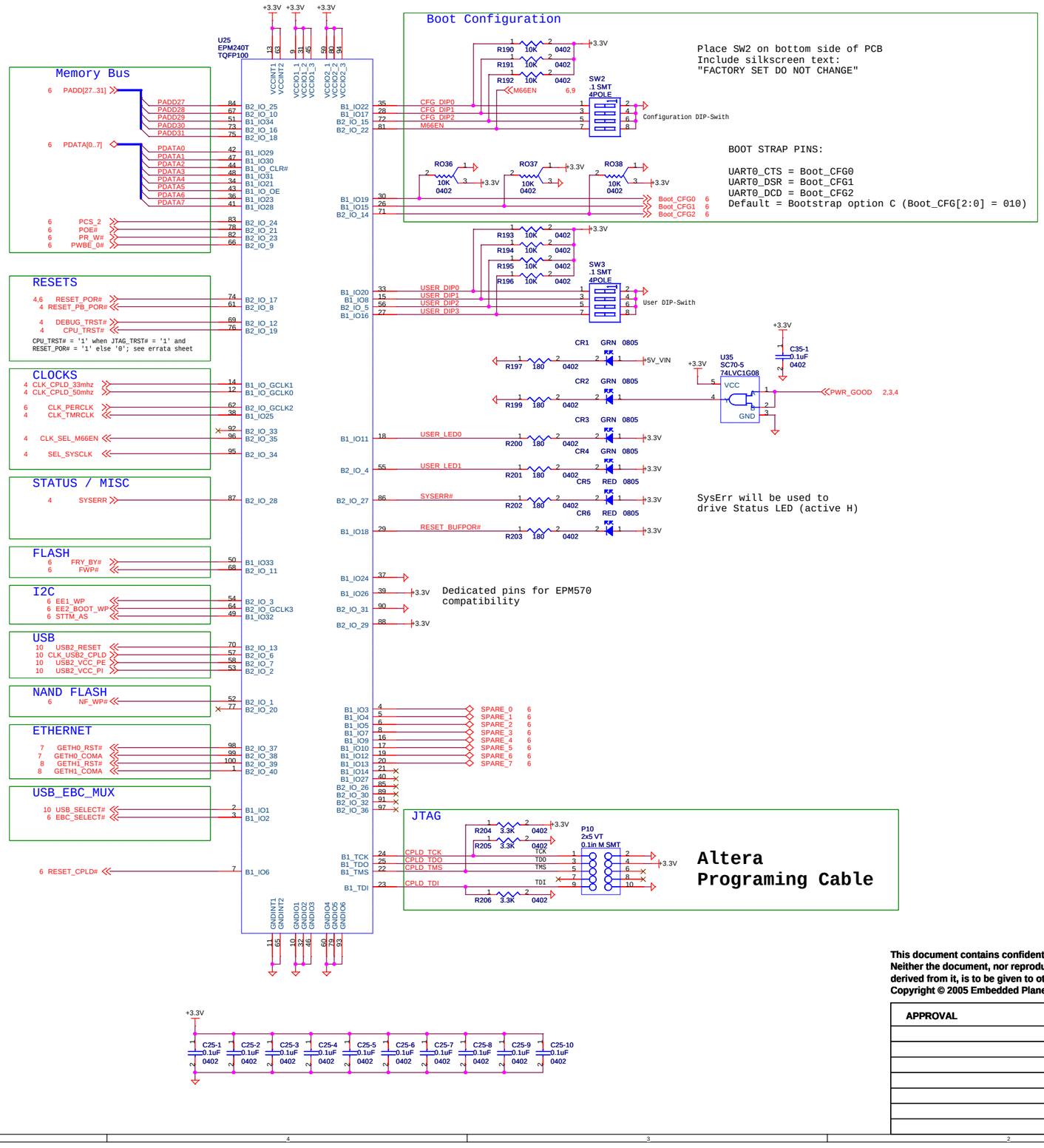
Page Name: USB
Title: Des0211_11
Size: Custom
Document Number: Des0211_11_sch_10
Rev: 1.0
Date: Thursday, September 07, 2006
Sheet 10 of 11



APPROVAL	DATE

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Page Name	CPLD
Title	Des0211_11
Size	Custom
Document Number	Des0211_11_sch_10
Rev	1.0
Date:	Wednesday, September 13, 2006
Sheet	11 of 11